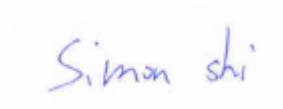
TEST REPORT

Engineering Recommendation G83 Issue 2 (December 2012)
Recommendations For The Connection Of Type Tested Small-Scale Embedded Generators (Up To 16A Per Phase) In Parallel With Low-Voltage Distribution Systems

Report reference No..... :	GZES180100090601
Tested by (printed name and signature) ..... :	Simon Shi 
Approved by (printed name and signature) ..... :	Roger Hu 
Date of issue ..... :	27 Jul 2017
Total pages..... :	76 pages
Testing Laboratory Name ..... :	SGS-CSTC Standards Technical Services Co., Ltd. - E&E Lab Guangzhou
Address ..... :	198 Kezhu Road, Scientech Park, Guangzhou Economic & Technology Development District, Guangzhou, Guangdong, China 510663
Testing location ..... :	Same as above
Address ..... :	Same as above
Applicant's Name ..... :	Shenzhen SOFARSOLAR Co., Ltd.
Address ..... :	5/F,Building 4, Antongda Industrial Park, No. 1 Liuxian Avenue, Xin'an Street, Bao'an District, Shenzhen City, Guangdong Province, P.R. China
Test specification	
Standard..... :	G83 Issue 2 : 2012
Test procedure ..... :	Type test
Non-standard test method ..... :	N/A
Test Report Form No. ..... :	G83/2a
TRF originator ..... :	Intertek
Master TRF ..... :	dated 2013-07
Test item description ..... :	Grid-connected inverter
Trademark ..... :	SOFAR SOLAR
Manufacturer ..... :	Same as applicant
Factory ..... :	Shenzhen SOFARSOLAR Co., Ltd. 5/F,Building 4, Antongda Industrial Park, No. 1 Liuxian Avenue, Xin'an Street, Bao'an District, Shenzhen City, Guangdong Province, P.R. China
Model and/or type reference ..... :	**SOFAR 3.6KTLM-G2, SOFAR 3KTLM-G2**

Rating(s) ..... :	DC input: 90-580V, 11/11A AC output: 230V, 50Hz, 16.0A, 3680VA (**SOFAR 3.6KTLM-G2)** AC output: 230V, 50Hz, 13.7A, 3000VA (**SOFAR 3KTLM-G2)** Software Version: V0.22

Summary of testing:

The sample(s) tested complied with the type test requirement of G83 Issue 2: 2012

Test case verdicts

Test case does not apply to the test object :	N/A
Test item does meet the requirement .....:	P(ass)
Test item does not meet the requirement ..:	F(ail)

Testing

Date of receipt of test item .....:	29th of November 2017
Date(s) of performance of test .....:	30th of November 2017 to 17th December of 2017

General remarks

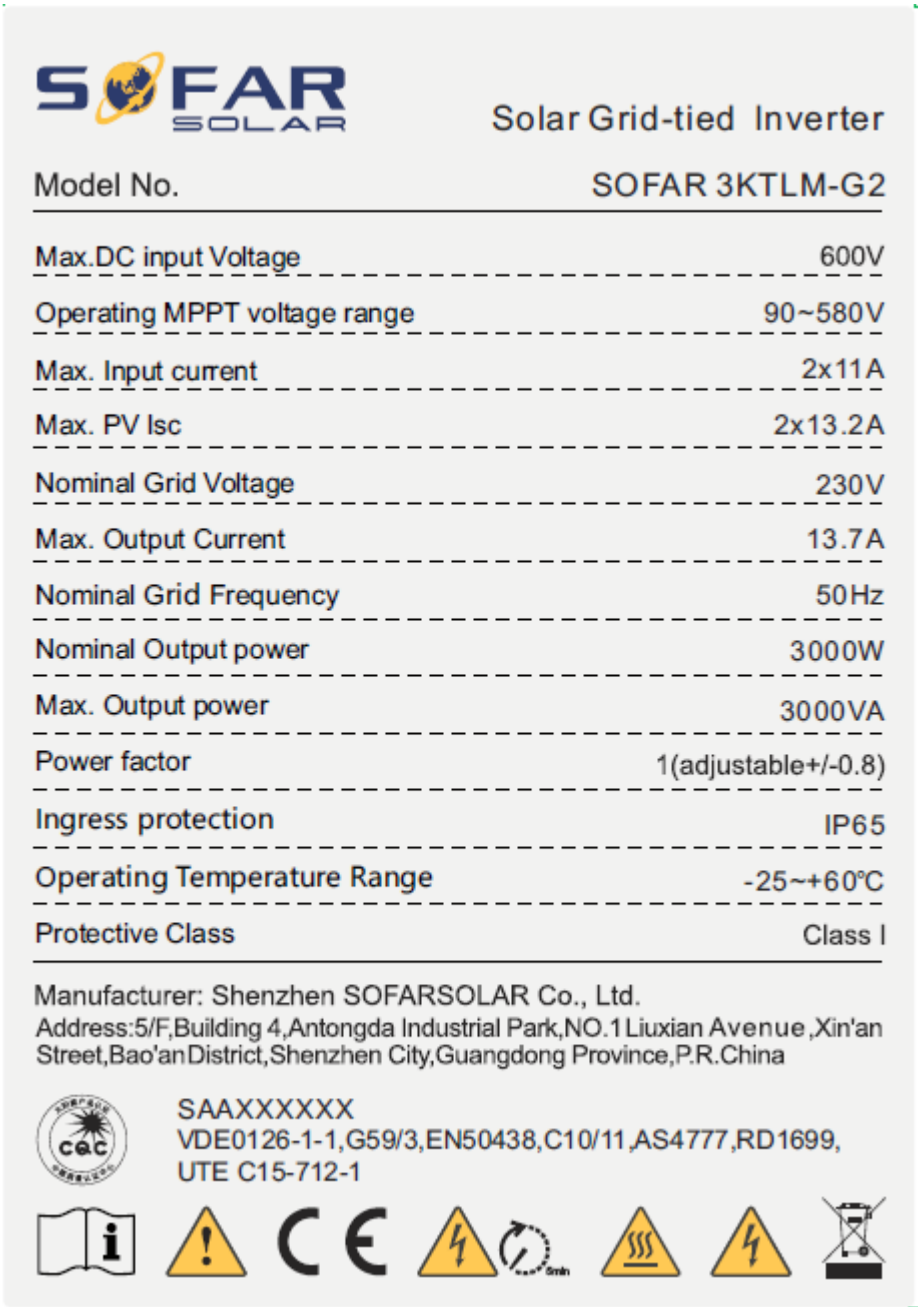
The test results presented in this report relate only to the object tested.
This report shall not be reproduced, except in full, without the written approval of the Issuing testing laboratory.
"(See Enclosure #)" refers to additional information appended to the report.
"(See appended table)" refers to a table appended to the report.

Throughout this report a point is used as the decimal separator.

General product information

The products covered by this report are a permanently-connected, in-door used utility-interactive and stand-alone inverter. It can take power from PV charger controller and batteries and convert it to AC power for the utility grid.

Copy of marking plate:



Note:

1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
2. Label is attached on the surface of enclosure and visible after installation
3. Labels of other models are as the same with **SOFAR 3KTLM-G2**'s except the parameters of rating.

Engineering recommendation G83/2			
Clause	Requirement – Test	Result – Remark	Verdict
5	Connection, Protection & Testing Requirements		P
5.1	Connection Procedure		N/A
5.2	Installation Wiring and Isolation		N/A
5.3	Interface Protection	Integrated into SSEG	P
5.3.1	Interface Protection Settings and Test Requirements	See table 5.3.1	P
	Interface Protection shall be installed which disconnects the SSEG system from the DNO's Distribution System when any parameter is outside of the settings shown in Table 1.		P
	The total disconnection time for voltage and frequency protection including the operating time of the disconnection device shall be the trip delay setting with a tolerance of, -0 s + 0.5s.		P
	All settings shall be applied as shown in the above table, so that they can be inspected if required by the DNO to confirm that the settings are correct.		P
	Only devices that have protection settings set and locked during manufacture can be considered as Type Tested		P
	The Manufacturer needs to establish a secure way of displaying the settings in one of the following ways.	The way (b) applied	P
	a) A display on a screen which can be read; b) A display on a PC which can communicate with the device and confirm that it is the correct device by means of a serial number permanently fixed to the device and visible on the PC screen at the same time as the settings; c) Display of all settings including nominal voltage and current outputs, alongside the serial number of the device, permanently fixed to the device.		P
	The Manufacturer must ensure that the Interface Protection is capable of measuring voltage to an accuracy of ± 1.5% of the nominal value (± 3.45V) and of measuring frequency to ± 0.2% of the nominal value (± 0.1Hz) across its operating range of voltage, frequency and temperature.	See table 5.3.1	P
	In response to a protection operation the SSEG system shall be automatically disconnected from the DNO's Distribution System, this disconnection must be achieved preferably by the separation of mechanical contacts or alternatively by the operation of a suitably rated solid state switching device.	Solid state switching device used	P
5.3.2	Loss of Mains Protection	See table 5.3.2 Test according to EN 62116	P

Engineering recommendation G83/2			
Clause	Requirement – Test	Result – Remark	Verdict
5.3.3	Frequency Drift and Step Change Stability Test	See table 5.3.3	P
5.3.4	Automatic Reconnection	See table 5.3.4	P
	the voltage and frequency on the DNO's Distribution System have remained within the limits of Table 1 for a minimum of 20 seconds		P
5.4	Quality of Supply		P
	the SSEG shall comply with the requirements of the EMC Directive and in particular the product family emission standards listed in Table 2.		P
5.4.1	Testing for Harmonic emissions	See table 5.4.1	P
5.4.2	Testing for flicker	See table 5.4.2	P
5.5	DC Injection	See table 5.5 and 5.6	P
	The upper limit for DC injection is 0.25% of AC current rating per phase		P
	Where necessary the DC emission requirements can also be satisfied by installing an isolating transformer between the Inverter and the connection to the DNO's Distribution System.		N/A
5.6	Power Factor	See table 5.5 and 5.6	P
	A power factor within the range 0.95 lagging to 0.95 leading	A Fixed power factor at range 0.95 lagging to 0.95 leading	P
5.7	Short Circuit Current Contribution	See table 5.7.2	--
5.7.1	Directly Coupled Generation	PV inverter	N/A
5.7.2	Inverter Connected Generation		P
5.8	Voltage Unbalance	Single phase	N/A
5.9	Certification Requirements		P
6	Operation and Safety	CE marking	P
6.1	Operational Requirements		N/A
6.2	Labelling		N/A
6.3	Maintenance & Routine Testing	This information including in the installation and user instructions	P
	Periodic testing of the SSEG is recommended at intervals prescribed by the Manufacturer. This information shall be included in the installation and User Instructions.		P
6.4	Earthing		P
7	Commissioning/Decommissioning and Acceptance Testing		N/A

Engineering recommendation G83/2			
Clause	Requirement – Test	Result – Remark	Verdict
Appendix 1	Connection Procedure Flow Chart		N/A
Appendix 2	Application for Connection		N/A
Appendix 3	SSEG Installation Commissioning Confirmation		N/A
Appendix 4	Type Verification Test Report		N/A
Appendix 5	SSEG Decommissioning Confirmation		N/A
Appendix 6	Relaxation of Commissioning Notification Timescales for SSEG: HSE Certificate of Exemption (August 2008)		N/A
Annex A1	Common Inverter Requirements.		P
A1.1	Certification & Type Testing SSEG Requirements		P
A1.2	CE Marking and Certification	A label with CE marking	P
A1.3	Type Verification Functional Testing of the Interface Protection		P
A1.3.1	Disconnection times		P
A1.3.2	Over / Under Voltage		P
A1.3.3	Over / Under Frequency		P
A1.3.4	Loss of Mains Protection		P
A1.3.5	Re-connection		P
A1.3.6	Frequency Drift and Step Change Stability test.		P
A1.4	POWER QUALITY		P
A1.4.1	Harmonics		P
A1.4.2	Power Factor		P
A1.4.3	Voltage Flicker		P
A1.4.4	DC Injection		P
A1.4.5	Overcurrent Protection		N/A
A1.4.6	Short Circuit Current Contribution		P
A1.4.7	Self-Monitoring - Solid State Disconnection		N/A
A1.4.8	Electromagnetic Compatibility (EMC)		P
Annex B1	Common Directly Coupled Connected SSEG Requirements		P
Annex C1	Separate Specific SSEG Technology Requirements		N/A
	C1.2 Photovoltaic		P

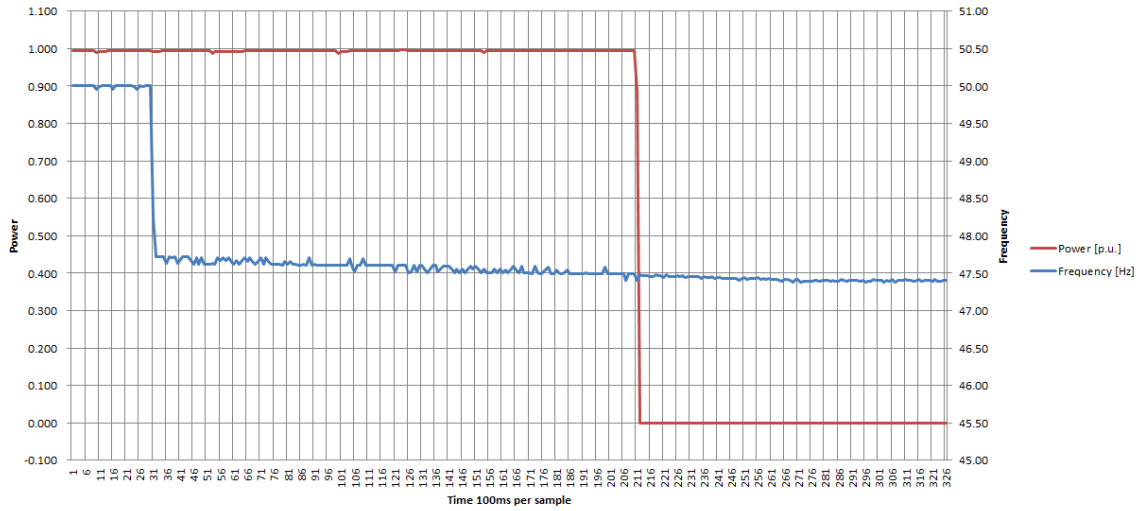
Appendix 1: Testing table

Table 5.3.1 Protection. Frequency tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2						**P**
Stage/Prot Function	Test	Frequency at the start (Hz)	Trip Frequency Desired (Hz)	Trip frequency measured (Hz)	Disconnection	Maximum deviation measured (Hz)
U/F st1 47.5 Hz	1	50	47.5	47.47	☐ NO ☒ YES	-0.03
	2	50	47.5	47.45	☐ NO ☒ YES	-0.05
	3	50	47.5	47.47	☐ NO ☒ YES	-0.03
	4	50	47.5	47.47	☐ NO ☒ YES	-0.03
	5	50	47.5	47.48	☐ NO ☒ YES	-0.02
U/f st2 47.0 Hz	1	50	47.0	46.93	☐ NO ☒ YES	-0.07
	2	50	47.0	46.94	☐ NO ☒ YES	-0.06
	3	50	47.0	46.94	☐ NO ☒ YES	-0.06
	4	50	47.0	46.95	☐ NO ☒ YES	-0.05
	5	50	47.0	46.93	☐ NO ☒ YES	-0.07
O/F st1 51.5 Hz	1	50	51.5	51.51	☐ NO ☒ YES	0.01
	2	50	51.5	51.50	☐ NO ☒ YES	0.00
	3	50	51.5	51.51	☐ NO ☒ YES	0.01
	4	50	51.5	51.49	☐ NO ☒ YES	-0.01
	5	50	51.5	51.50	☐ NO ☒ YES	0.00
O/F st2 52.0 Hz	1	50	52.0	52.06	☐ NO ☒ YES	0.06
	2	50	52.0	52.06	☐ NO ☒ YES	0.06
	3	50	52.0	52.07	☐ NO ☒ YES	0.07
	4	50	52.0	52.08	☐ NO ☒ YES	0.08
	5	50	52.0	52.08	☐ NO ☒ YES	0.08

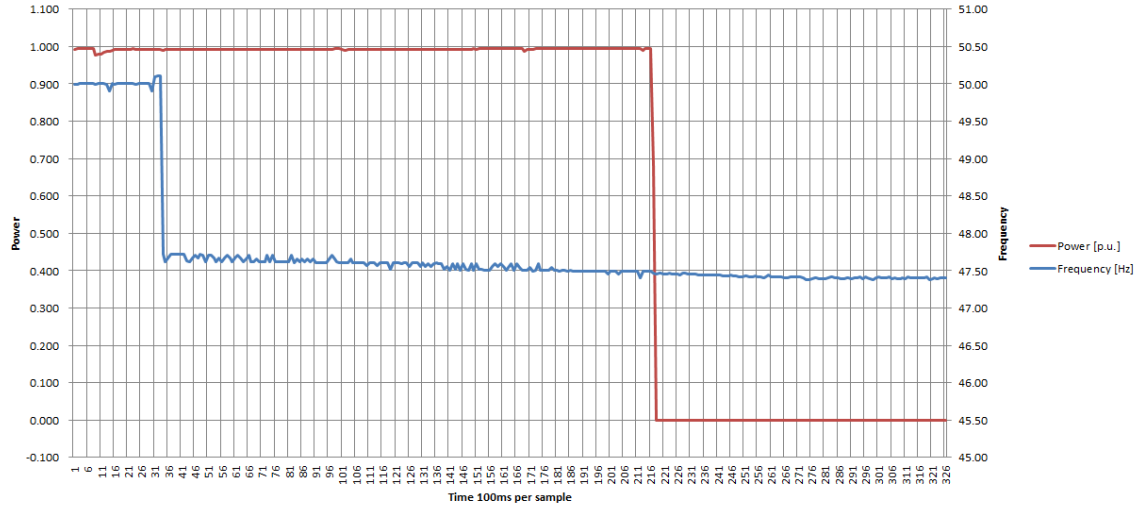
Appendix 1: Testing table

Test results are graphically shown in following pages.

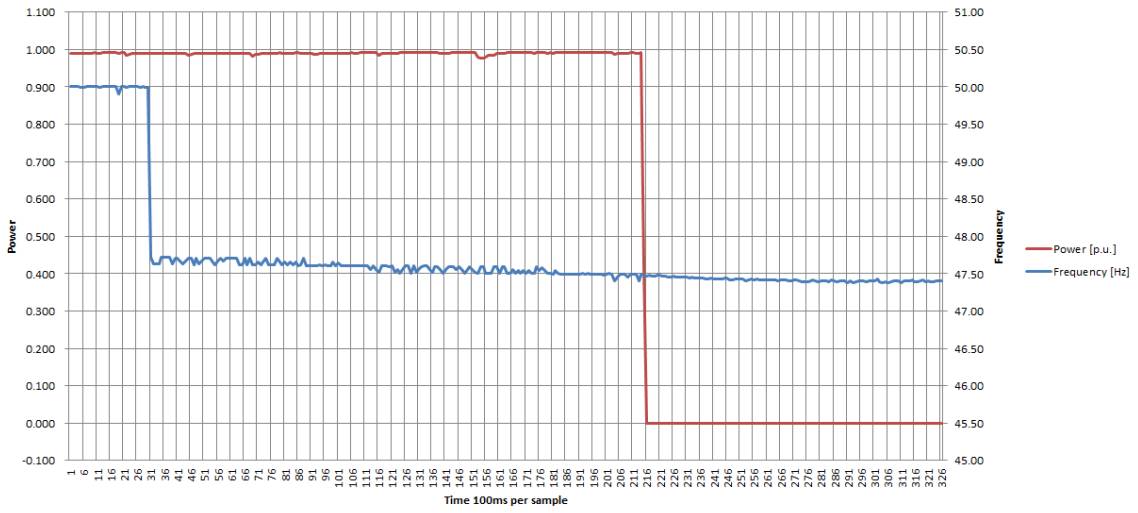
Under frequency, Stage 1 - Test 1



Under frequency, Stage 1 - Test 2



Appendix 1: Testing table

Under frequency, Stage 1 - Test 3


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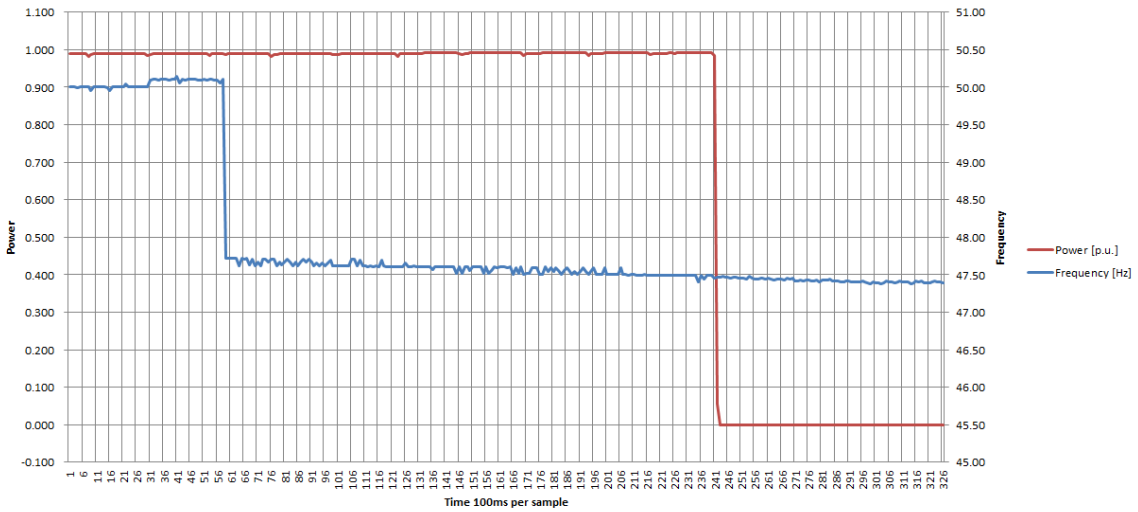
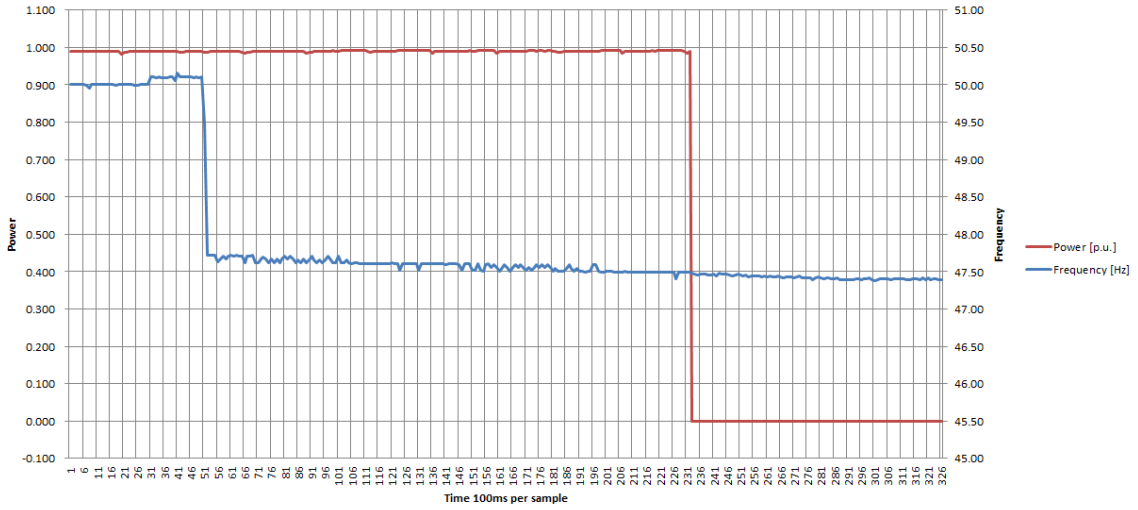
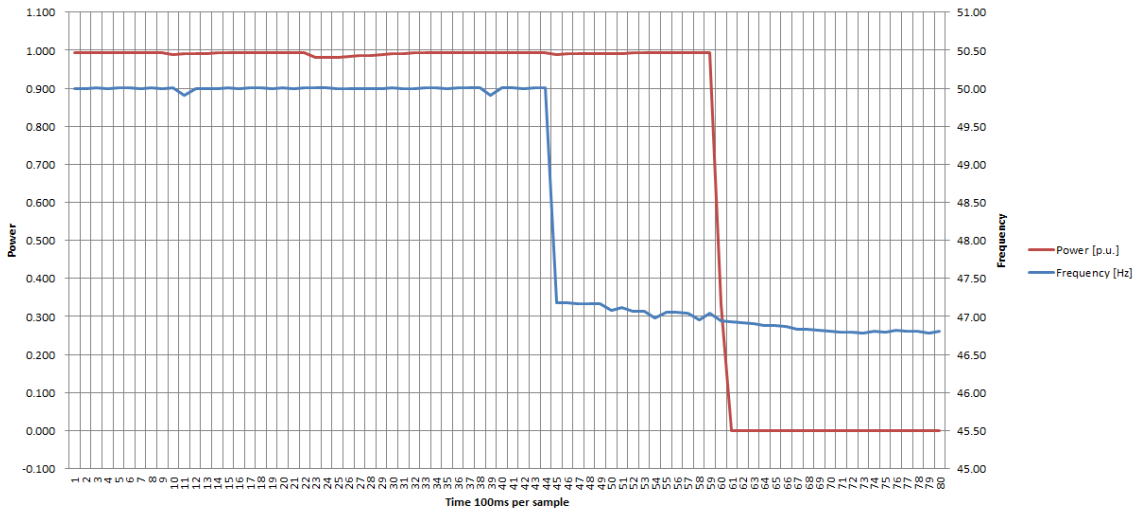


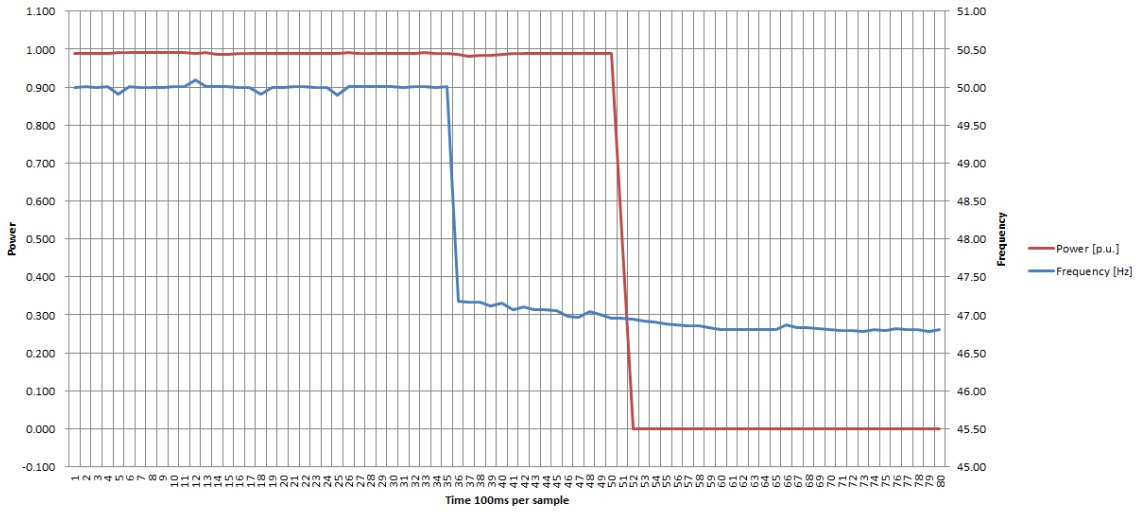
Appendix 1: Testing table

Under frequency, Stage 1 - Test 5


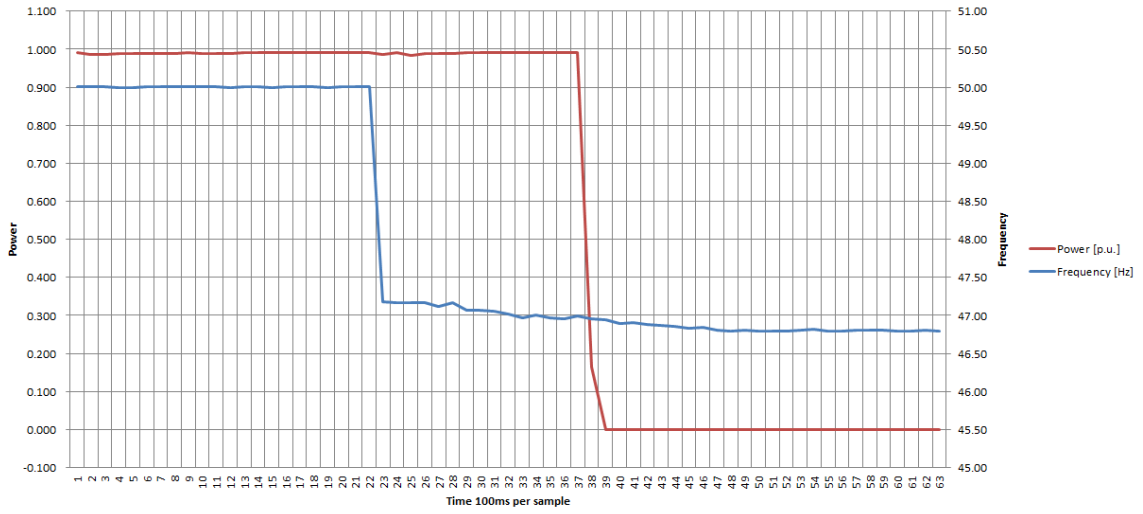
Under frequency, Stage 2 - Test 1


Appendix 1: Testing table

Under frequency, Stage 2 - Test 2

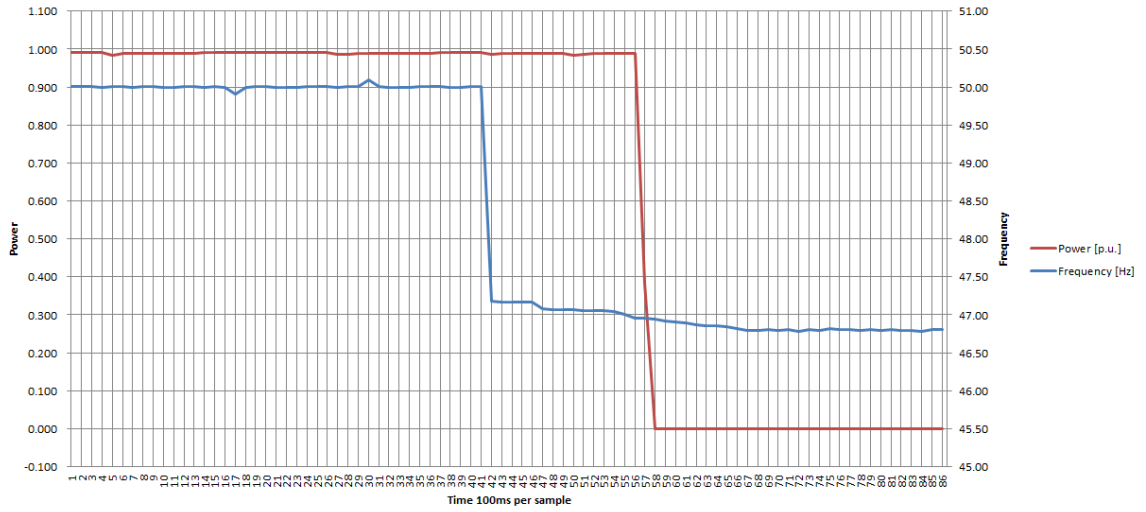


Under frequency, Stage 2 - Test 3

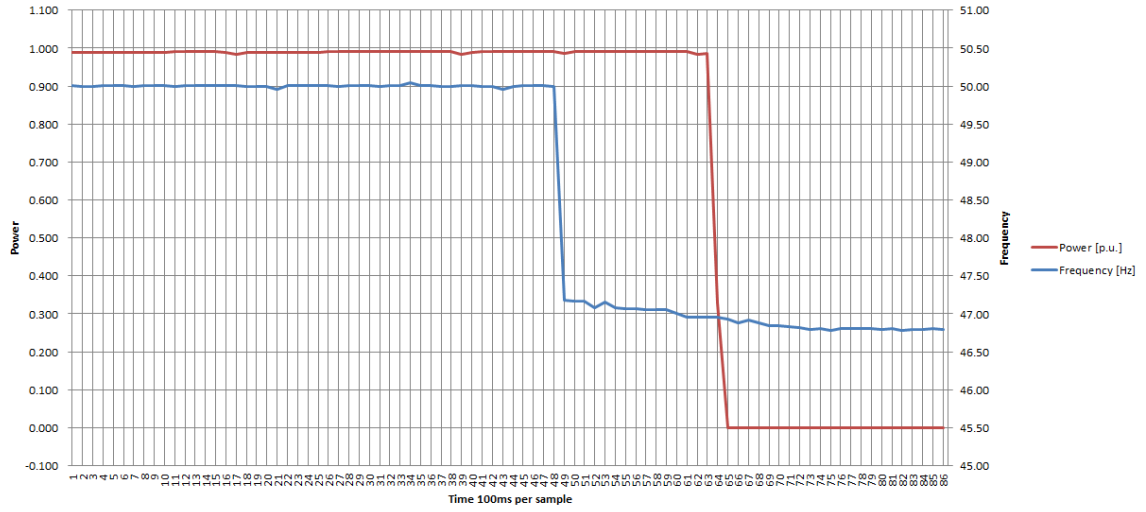


Appendix 1: Testing table

Under frequency, Stage 2 - Test 4

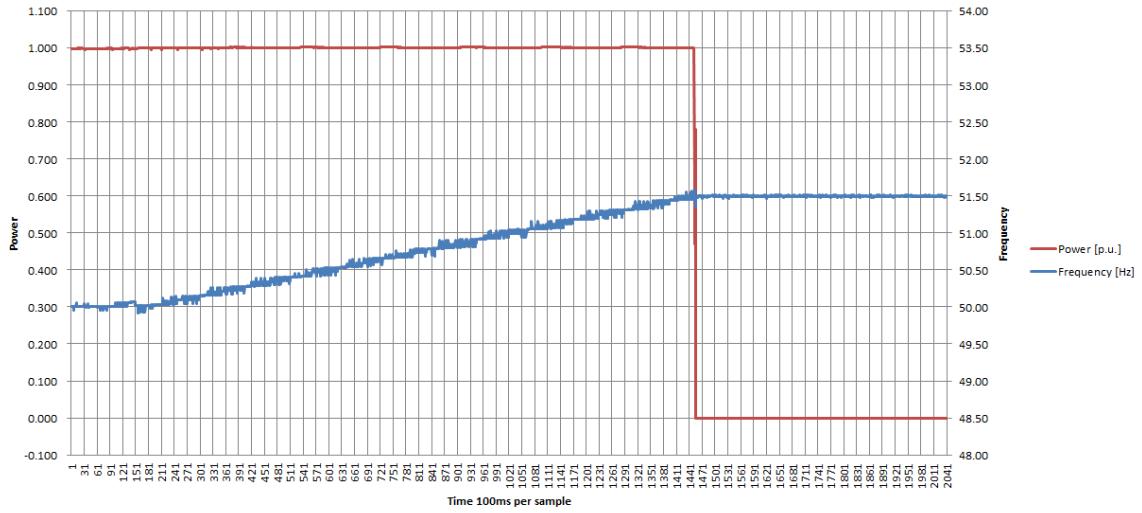


Under frequency, Stage 2 - Test 5

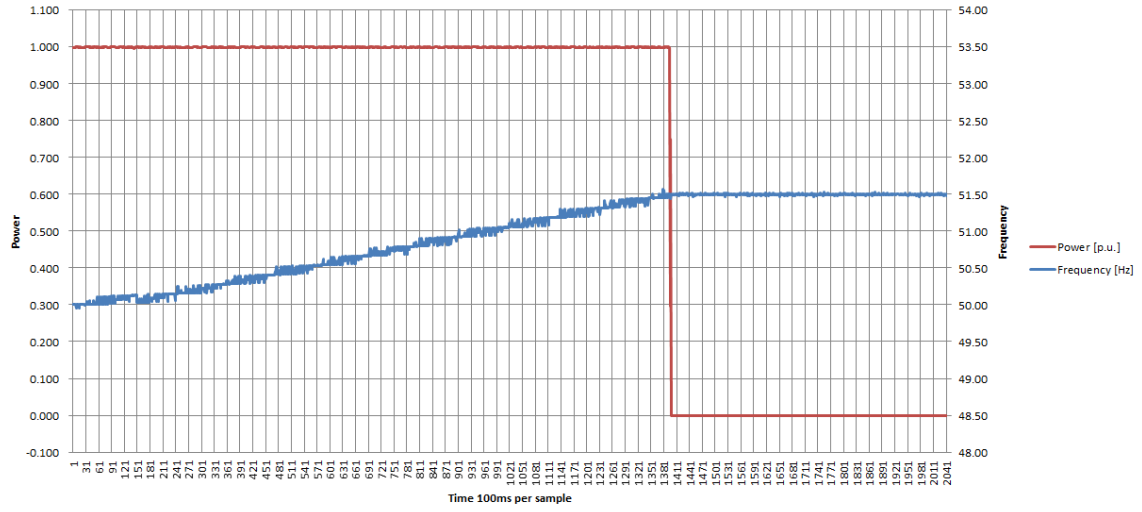


Appendix 1: Testing table

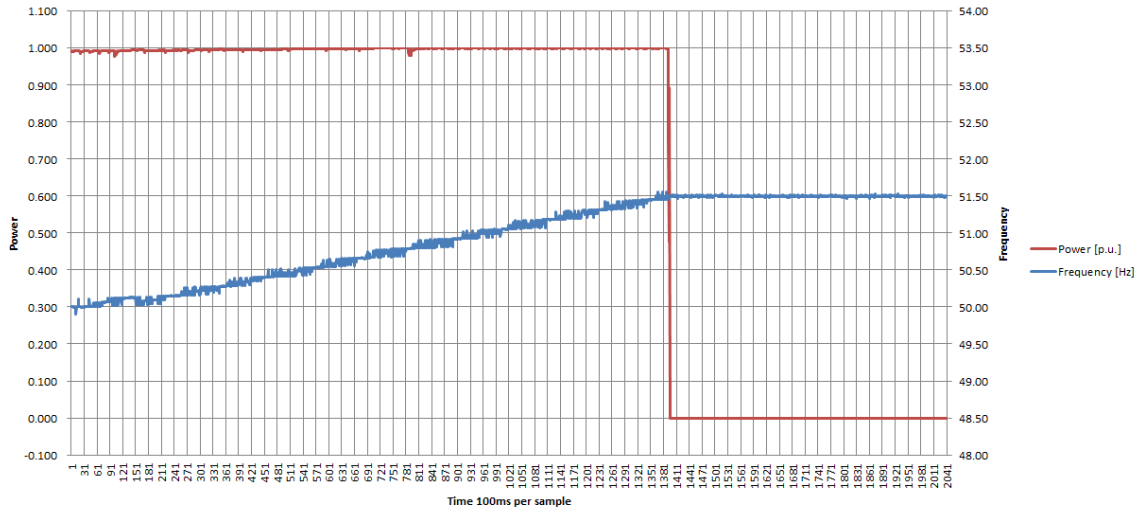
Over frequency, Stage 1 - Test 1



Over frequency, Stage 1 - Test 2



Appendix 1: Testing table

Over frequency, Stage 1 - Test 3


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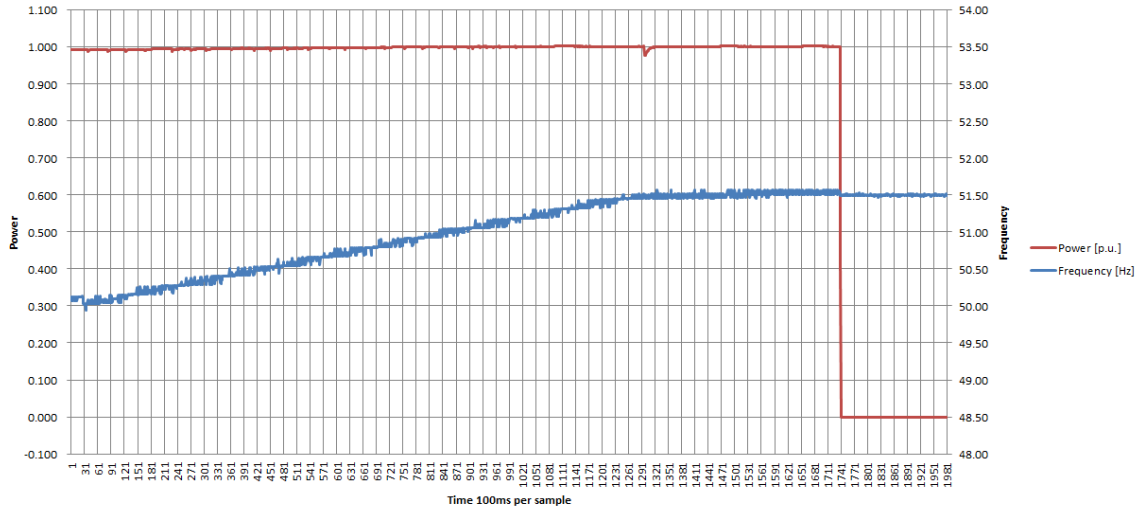
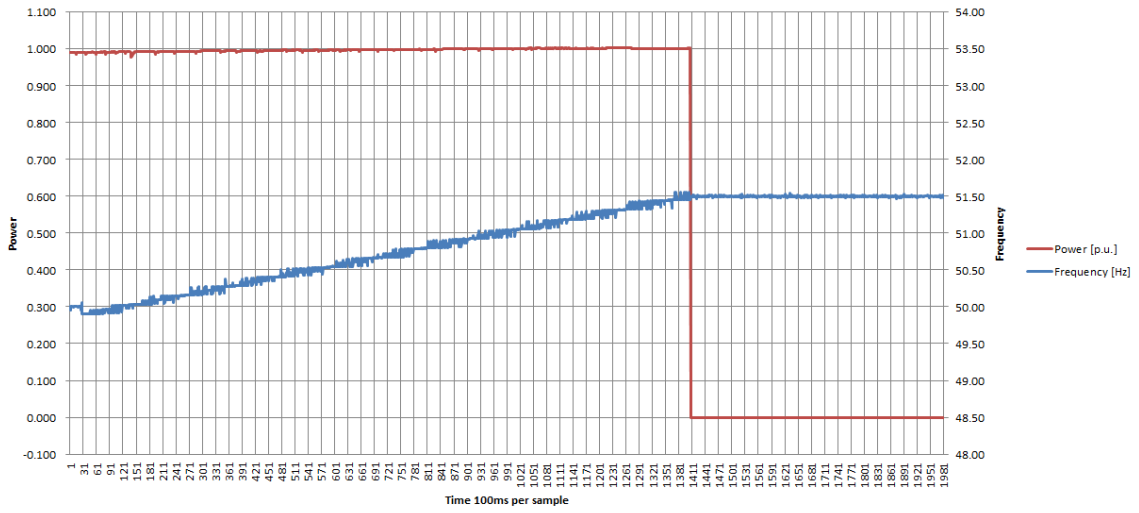
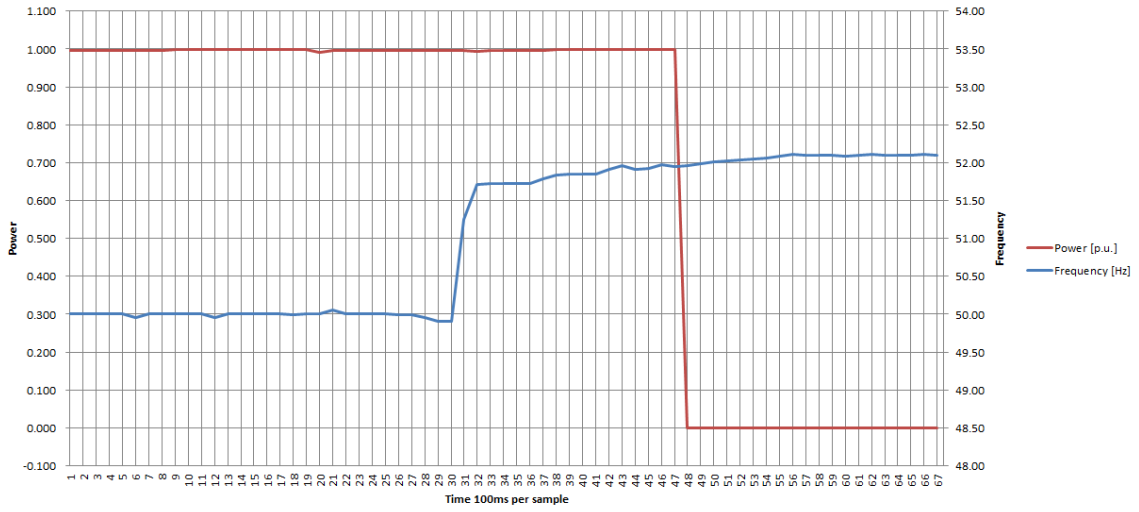


Appendix 1: Testing table

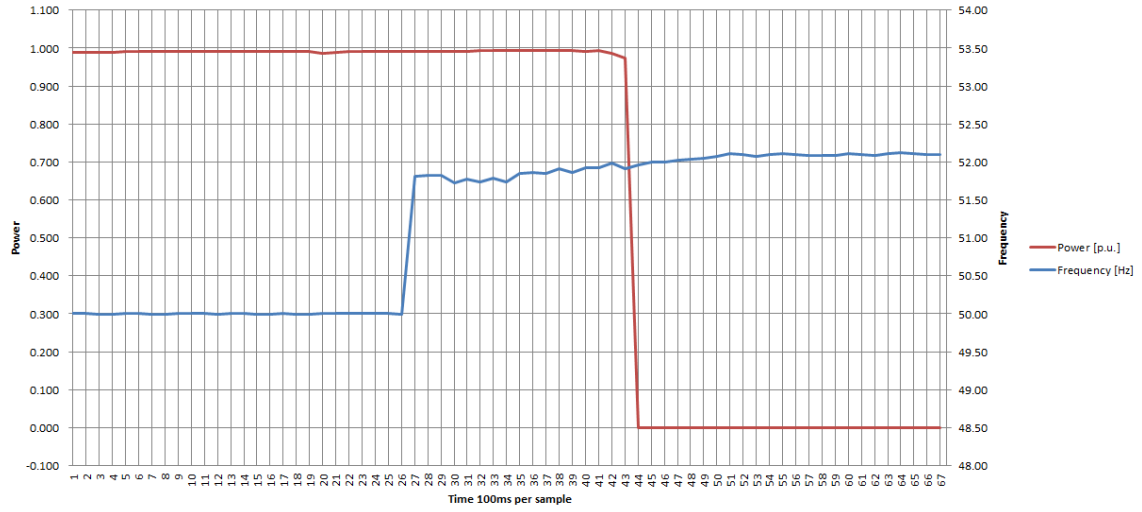
Over frequency, Stage 1 - Test 5



Over frequency, Stage 2 - Test 1



Appendix 1: Testing table

Over frequency, Stage 2 - Test 2


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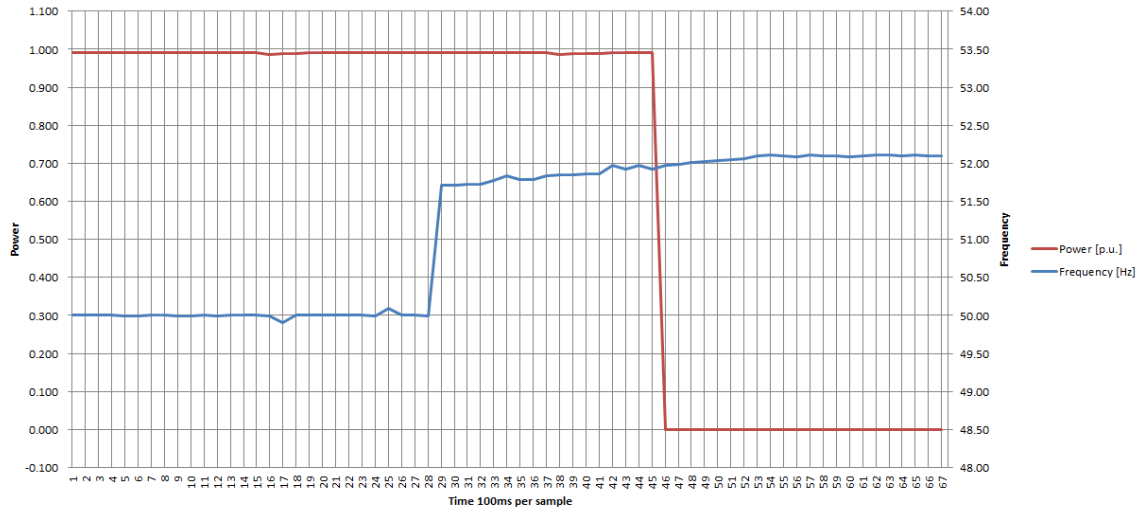
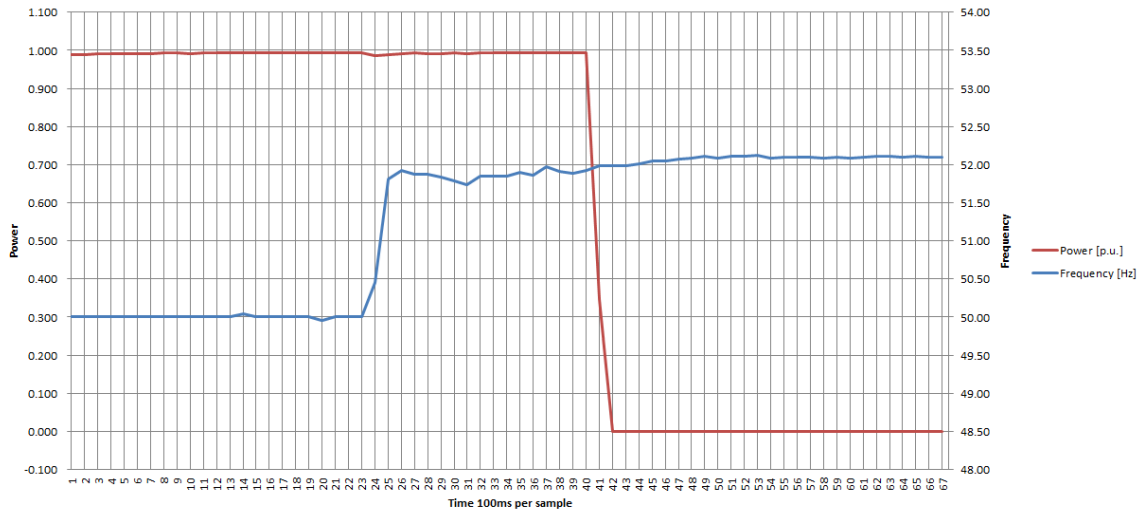


Appendix 1: Testing table

Over frequency, Stage 2 - Test 4


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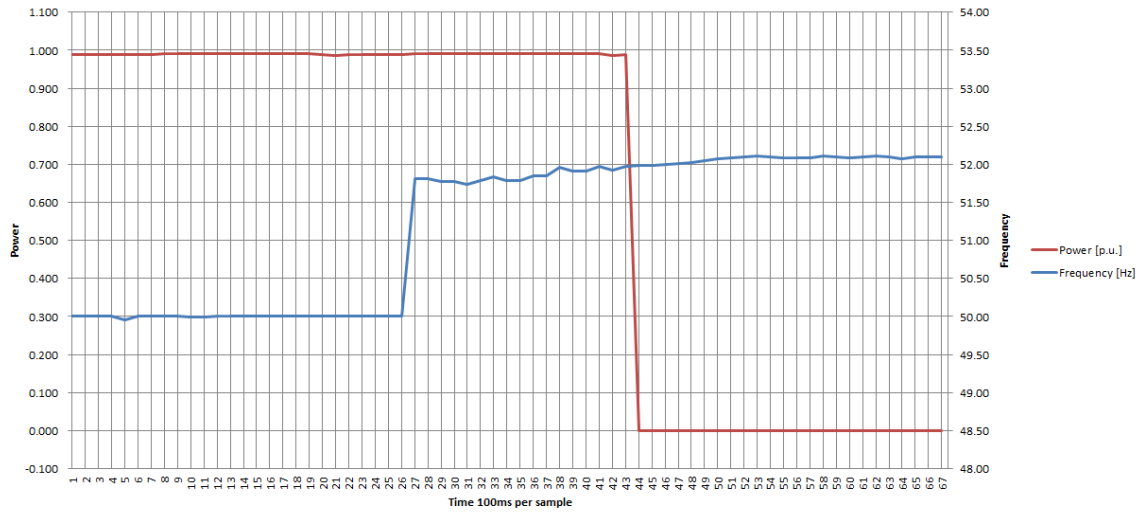


Appendix 1: Testing table

Trip time test.

The tests have been made as the following procedure:

- For underfrequency protection: Starting from a frequency level above the trip value of the protection function to be tested, the frequency is decreased in a step to a value below the frequency setpoint of the protection function and it´s measured from that instant the time it takes to disconnect.
- For overfrequency protection: Starting from a frequency level below the trip value of the protection function to be tested, the frequency is increased in a step to a value above the frequency setpoint of the protection function and it´s measured from that instant the time it takes to disconnect.

The tests have been performed at rated power. Each protection function has been tested 5 times.

Following tables show the test results.

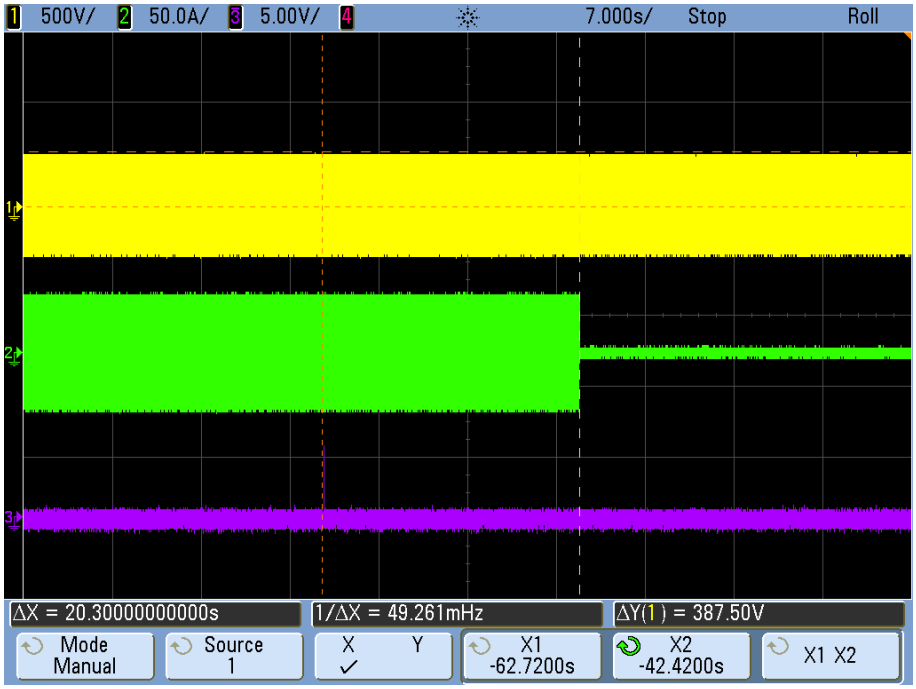
Appendix 1: Testing table

Table 5.3.1 Protection. Frequency tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2					**P**
Stage/Prot Function	Test	Delay Time limit (s)	Maximum trip time (s)	Trip time measured (s)	Disconnection
U/F st1 47.5 Hz	1	20	20.5	20.300	☐ NO ☒ YES
	2	20	20.5	20.230	☐ NO ☒ YES
	3	20	20.5	20.300	☐ NO ☒ YES
	4	20	20.5	20.370	☐ NO ☒ YES
	5	20	20.5	20.300	☐ NO ☒ YES
U/f st2 47.0 Hz	1	0.5	1.0	0.646	☐ NO ☒ YES
	2	0.5	1.0	0.669	☐ NO ☒ YES
	3	0.5	1.0	0.657	☐ NO ☒ YES
	4	0.5	1.0	0.660	☐ NO ☒ YES
	5	0.5	1.0	0.648	☐ NO ☒ YES
O/F st1 51.5 Hz	1	90	90.5	90.300	☐ NO ☒ YES
	2	90	90.5	90.320	☐ NO ☒ YES
	3	90	90.5	90.360	☐ NO ☒ YES
	4	90	90.5	90.370	☐ NO ☒ YES
	5	90	90.5	90.306	☐ NO ☒ YES
O/F st2 52.0 Hz	1	0.5	1.0	0.516	☐ NO ☒ YES
	2	0.5	1.0	0.536	☐ NO ☒ YES
	3	0.5	1.0	0.544	☐ NO ☒ YES
	4	0.5	1.0	0.532	☐ NO ☒ YES
	5	0.5	1.0	0.516	☐ NO ☒ YES

Appendix 1: Testing table

Test results are graphically shown in following pages.

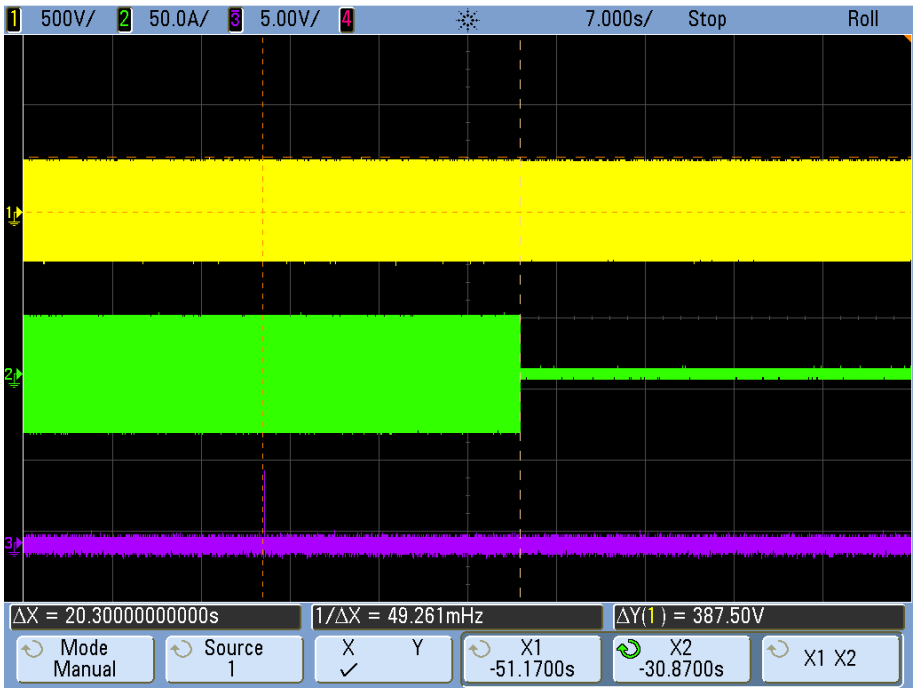
Under frequency, Stage 1 - Test 1



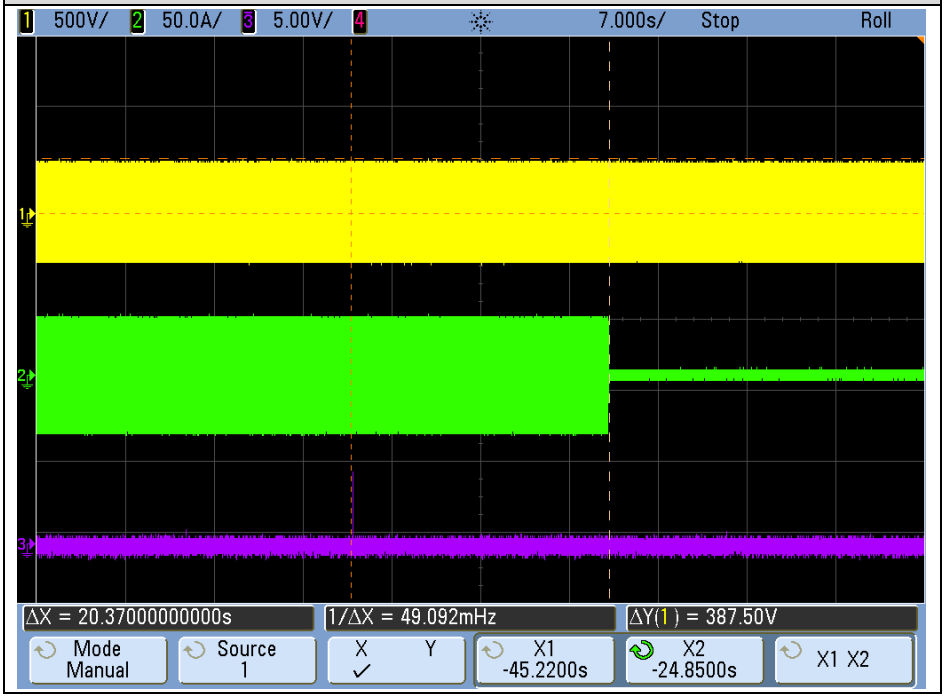
Under frequency, Stage 1 - Test 2

Appendix 1: Testing table

Under frequency, Stage 1 - Test 3

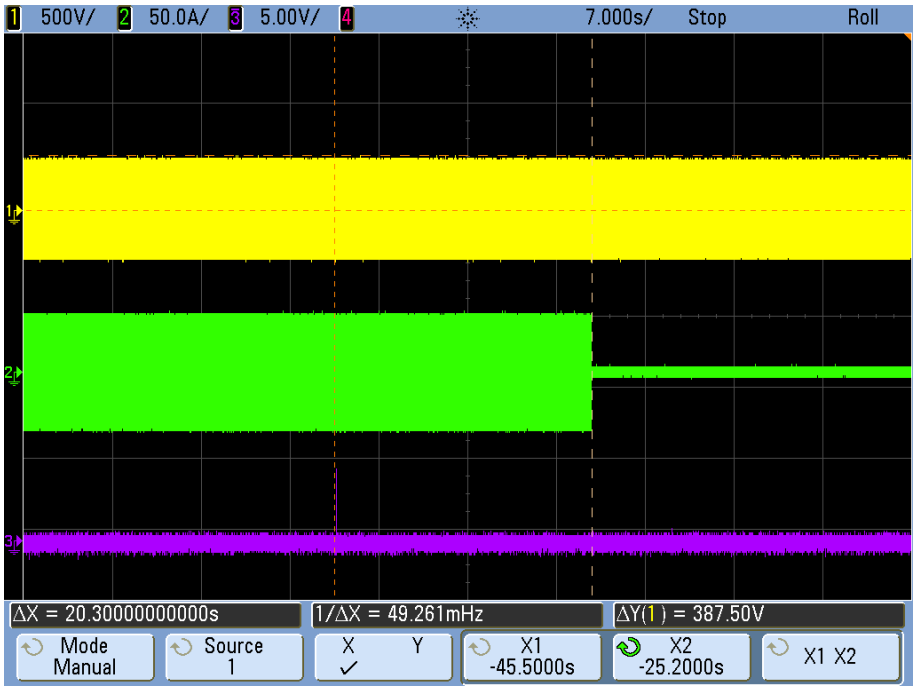


Under frequency, Stage 1 - Test 4

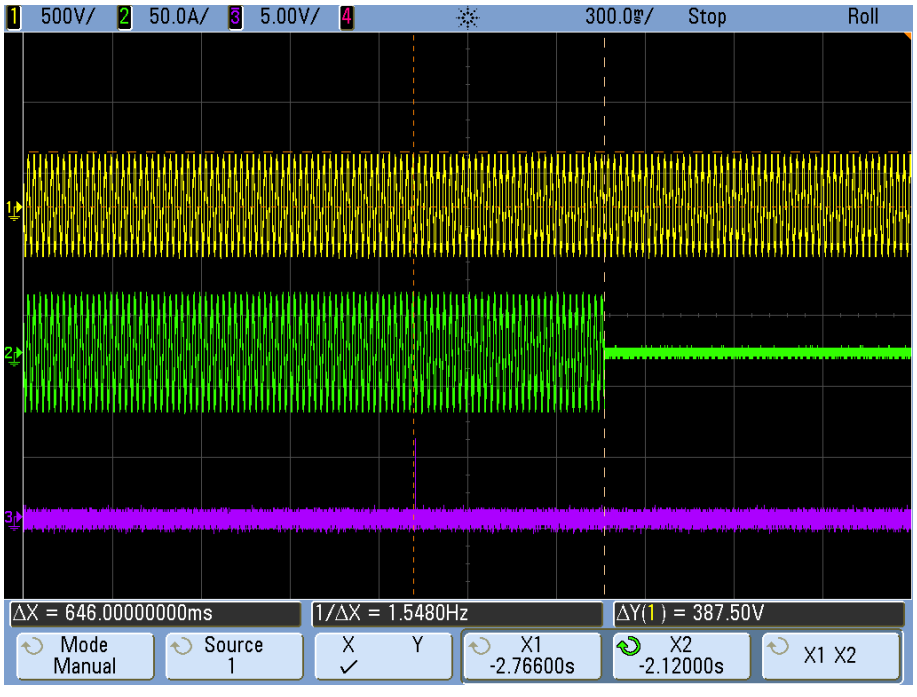


Appendix 1: Testing table

Under frequency, Stage 1 - Test 5

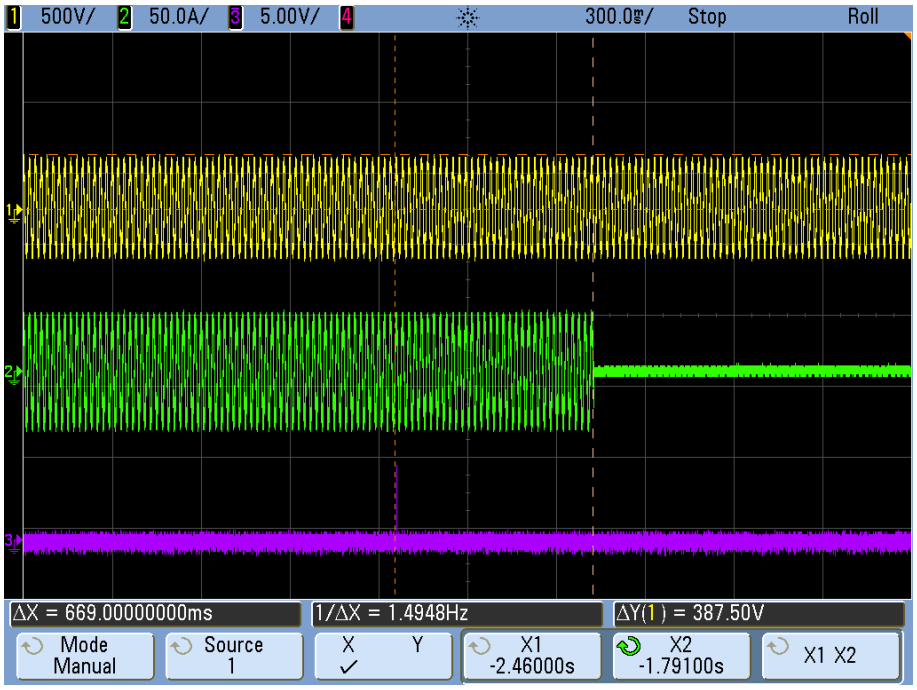


Under frequency, Stage 2 - Test 1

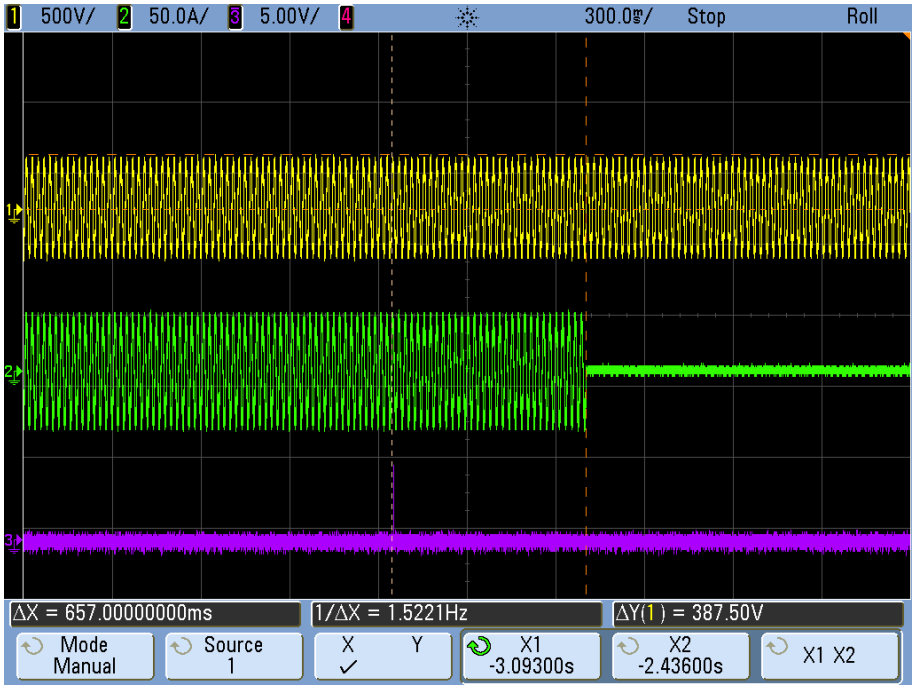


Appendix 1: Testing table

Under frequency, Stage 2 - Test 2

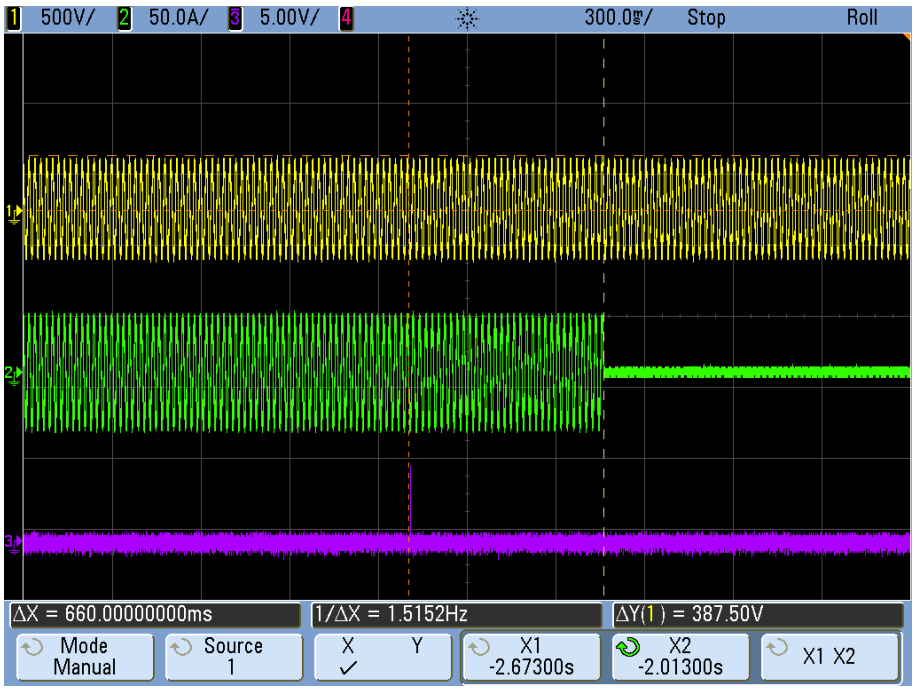


Under frequency, Stage 2 - Test 3

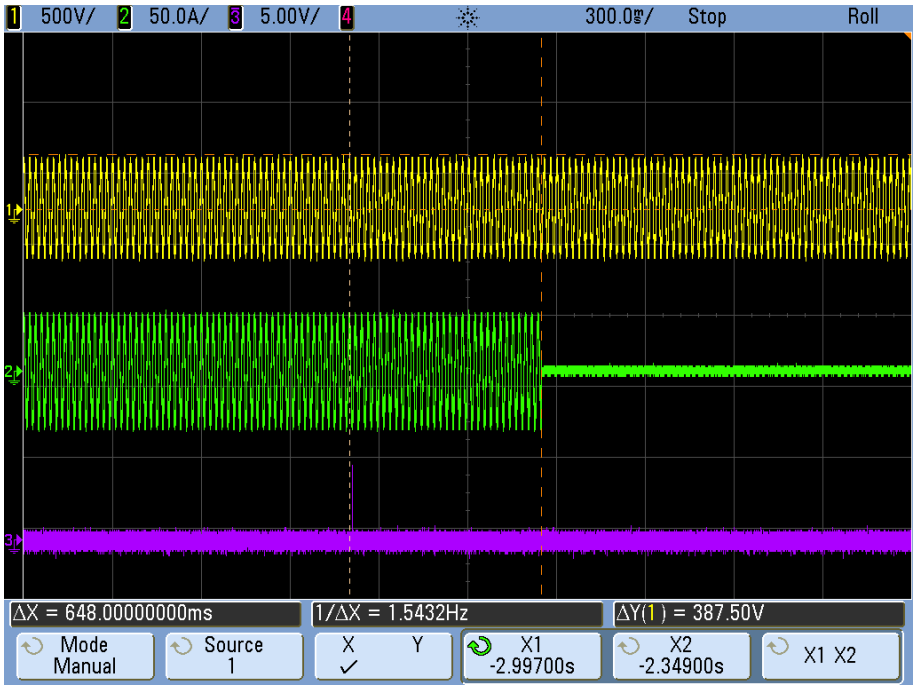


Appendix 1: Testing table

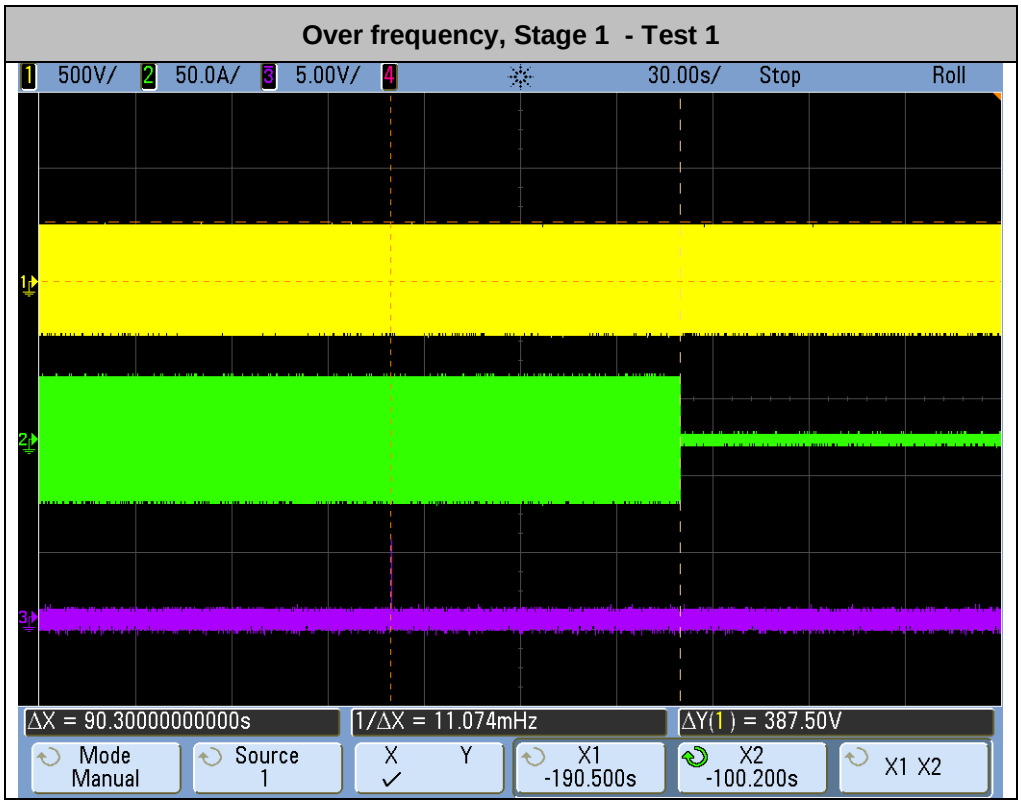
Under frequency, Stage 2 - Test 4

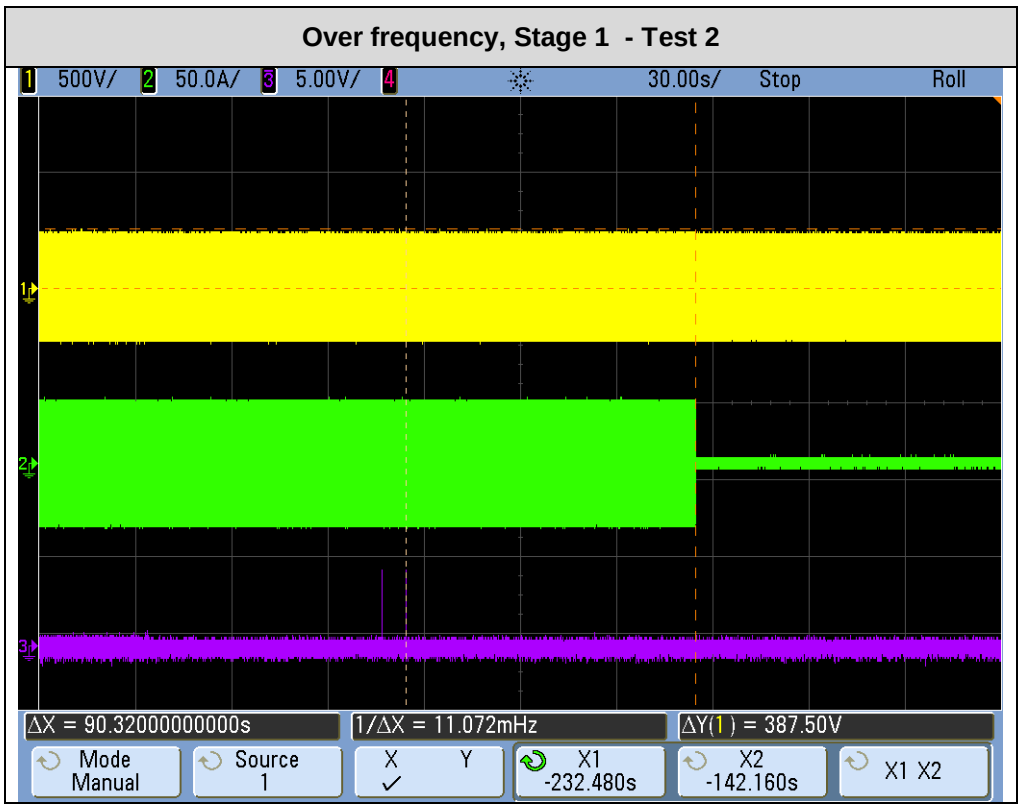


Under frequency, Stage 2 - Test 5



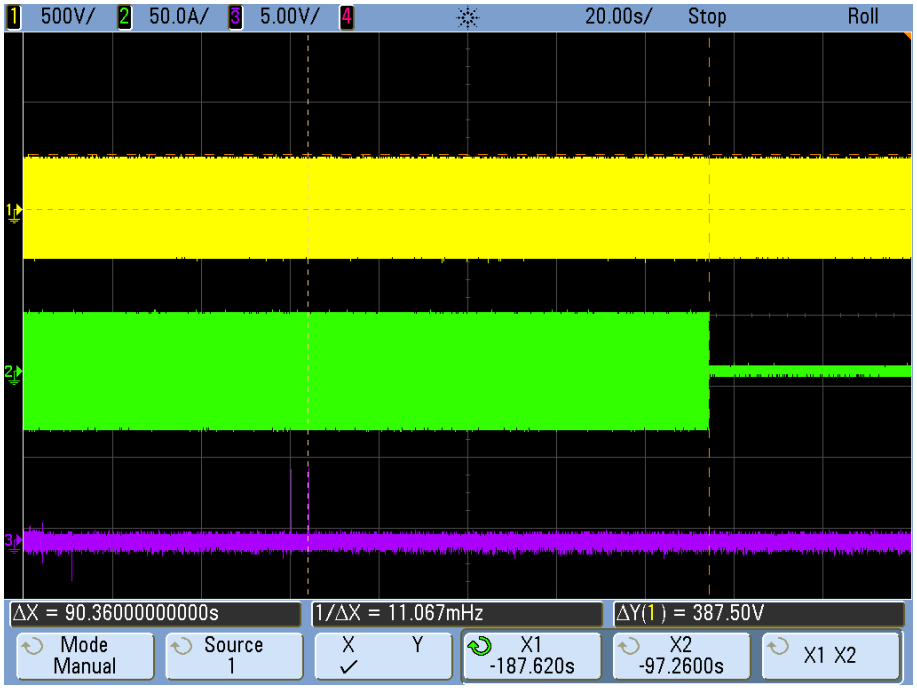
Appendix 1: Testing table



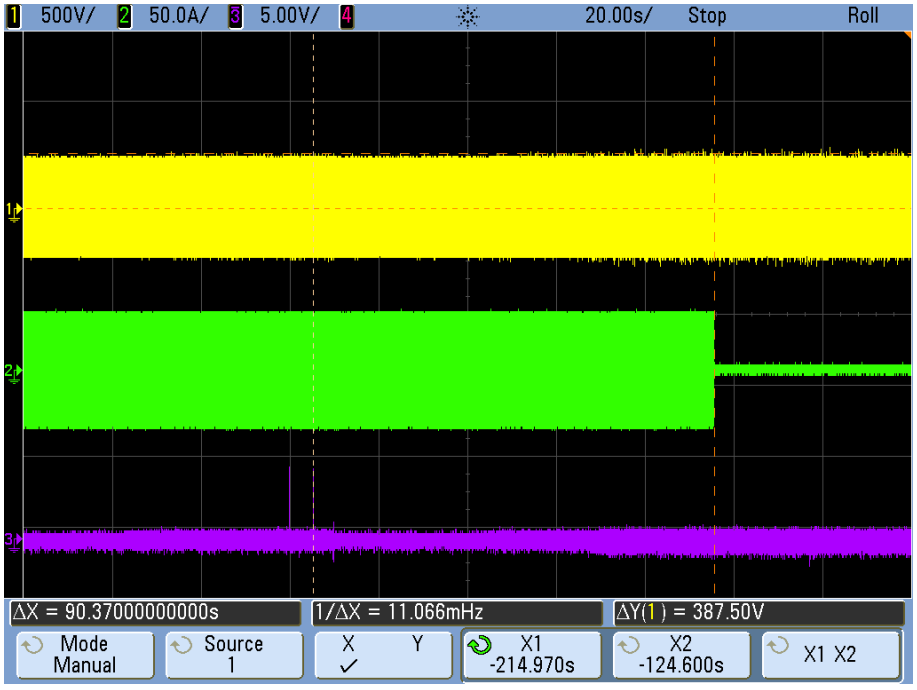


Appendix 1: Testing table

Over frequency, Stage 1 - Test 3

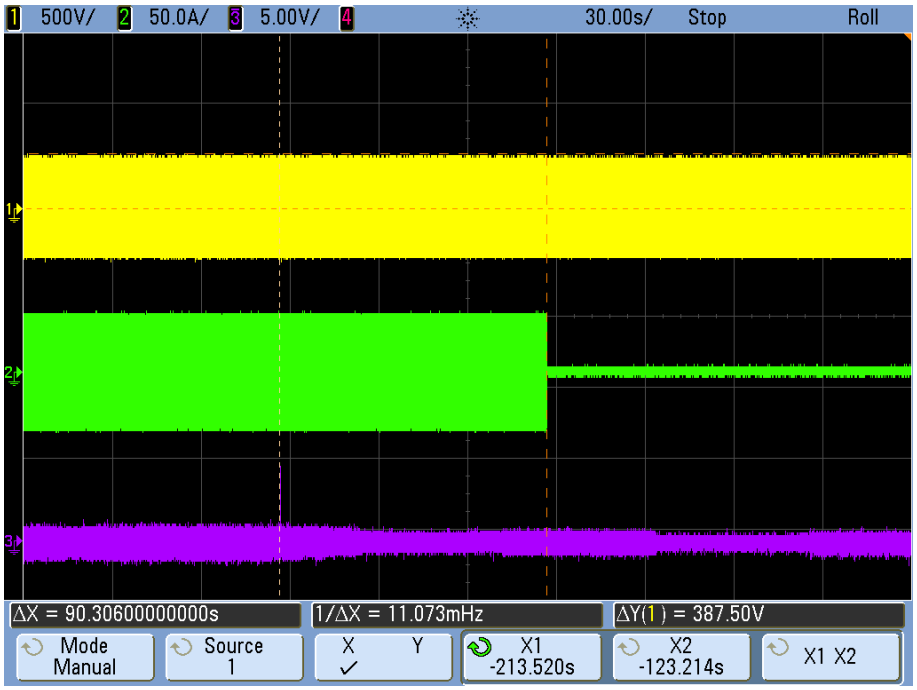


Over frequency, Stage 1 - Test 4

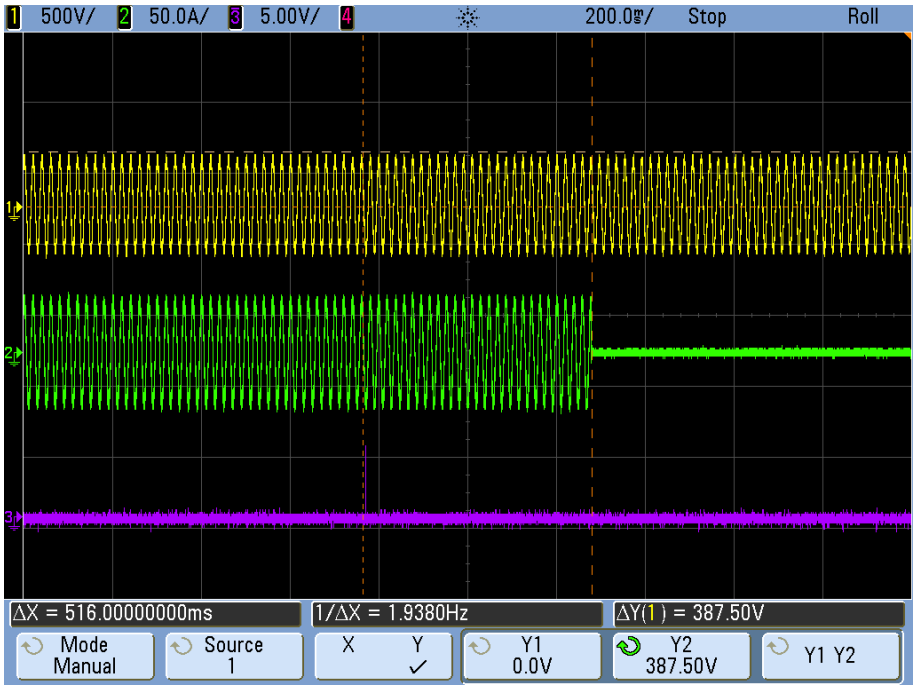


Appendix 1: Testing table

Over frequency, Stage 1 - Test 5

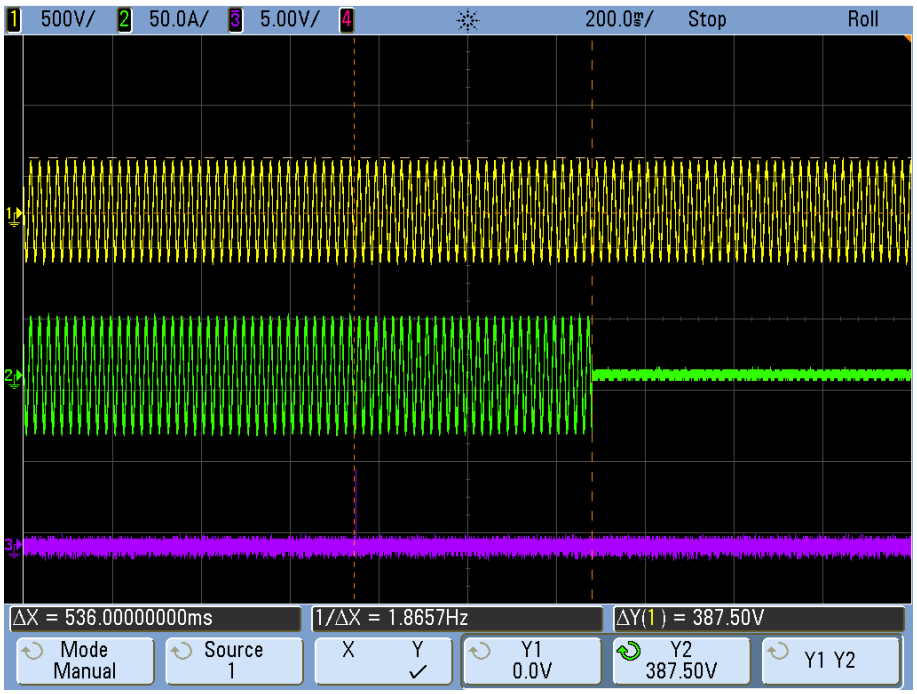


Over frequency, Stage 2 - Test 1

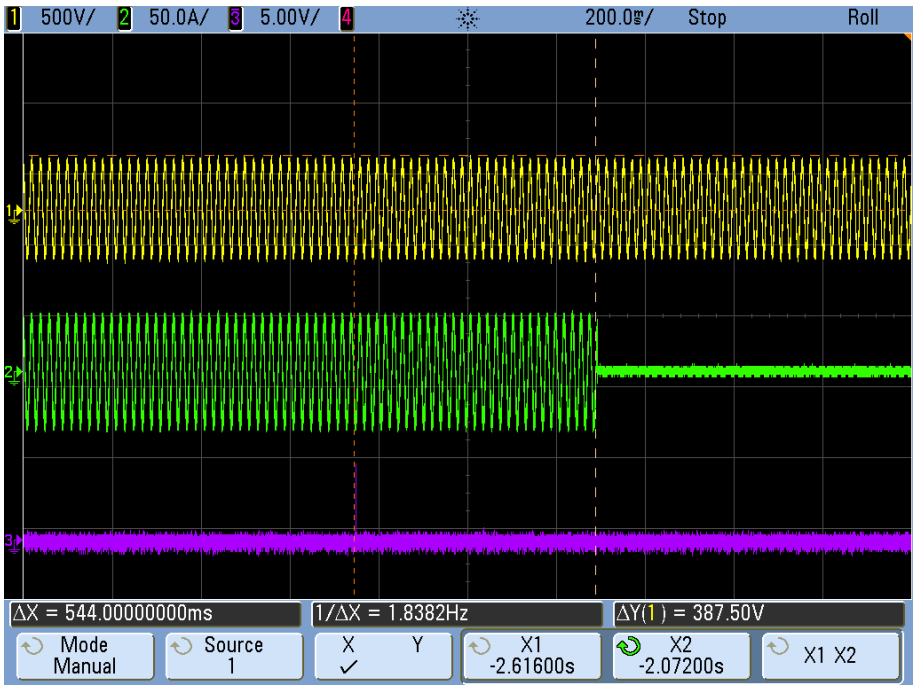


Appendix 1: Testing table

Over frequency, Stage 2 - Test 2



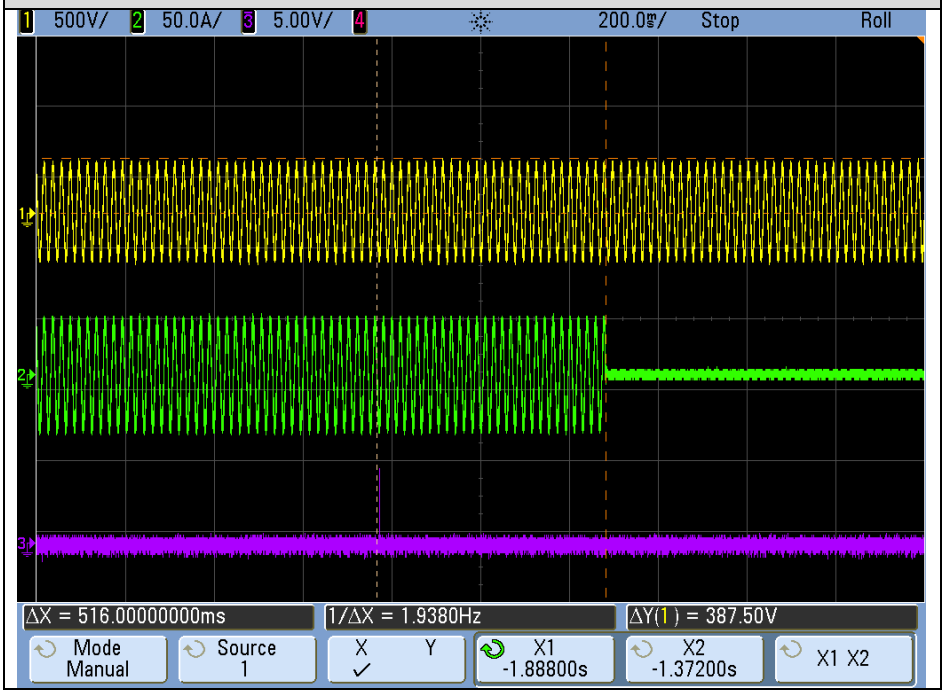
Over frequency, Stage 2 - Test 3



Appendix 1: Testing table

Over frequency, Stage 2 - Test 4

Over frequency, Stage 2 - Test 5



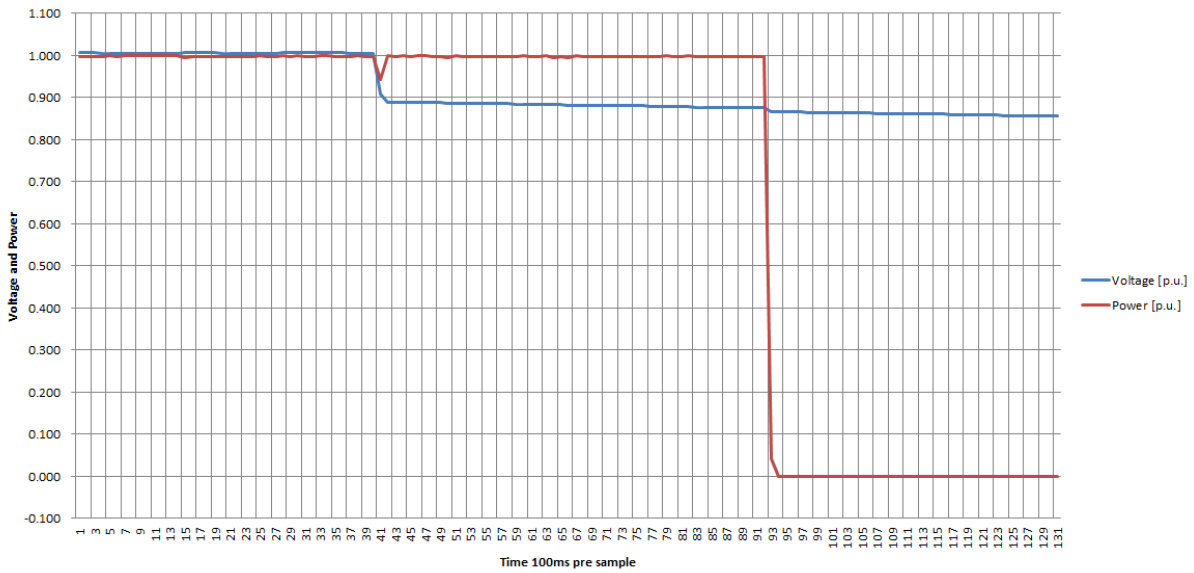
Appendix 1: Testing table

Table 5.3.1 (Continue) Protection. Voltage tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2						P
Stage/Prot Function	Test	Voltage at the start (V)	Trip Voltage Desired (V)	Trip voltage measured (V)	Disconnection	Deviation measured (%Un)
U/V st1 87% Un	1	230	200.1	199.22	☐ NO ☒ YES	-0.383
	2	230	200.1	199.26	☐ NO ☒ YES	-0.365
	3	230	200.1	199.42	☐ NO ☒ YES	-0.296
	4	230	200.1	199.36	☐ NO ☒ YES	-0.322
	5	230	200.1	199.13	☐ NO ☒ YES	-0.422
U/V st2 80% Un	1	230	184.0	183.92	☐ NO ☒ YES	-0.035
	2	230	184.0	183.97	☐ NO ☒ YES	-0.013
	3	230	184.0	184.01	☐ NO ☒ YES	0.004
	4	230	184.0	183.98	☐ NO ☒ YES	-0.009
	5	230	184.0	184.08	☐ NO ☒ YES	0.035
O/V st1 114% Un	1	230	262.2	262.84	☐ NO ☒ YES	0.278
	2	230	262.2	262.59	☐ NO ☒ YES	0.170
	3	230	262.2	262.93	☐ NO ☒ YES	0.317
	4	230	262.2	262.64	☐ NO ☒ YES	0.191
	5	230	262.2	262.58	☐ NO ☒ YES	0.165
O/V st2 119% Un	1	230	273.7	273.90	☐ NO ☒ YES	0.087
	2	230	273.7	273.93	☐ NO ☒ YES	0.100
	3	230	273.7	273.98	☐ NO ☒ YES	0.122
	4	230	273.7	273.95	☐ NO ☒ YES	0.109
	5	230	273.7	274.01	☐ NO ☒ YES	0.135

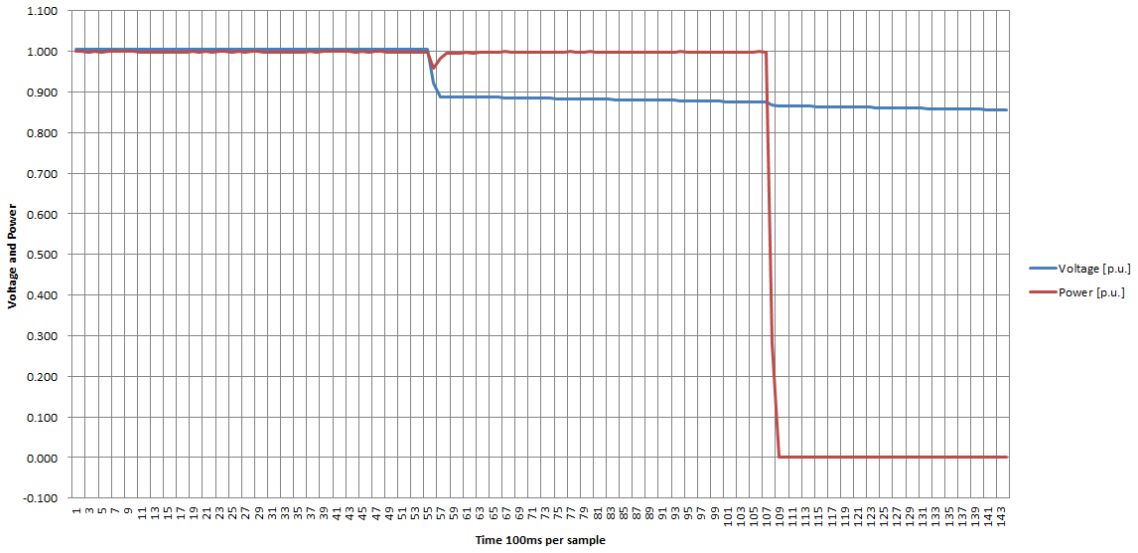
Appendix 1: Testing table

Test results are graphically shown in following pages.

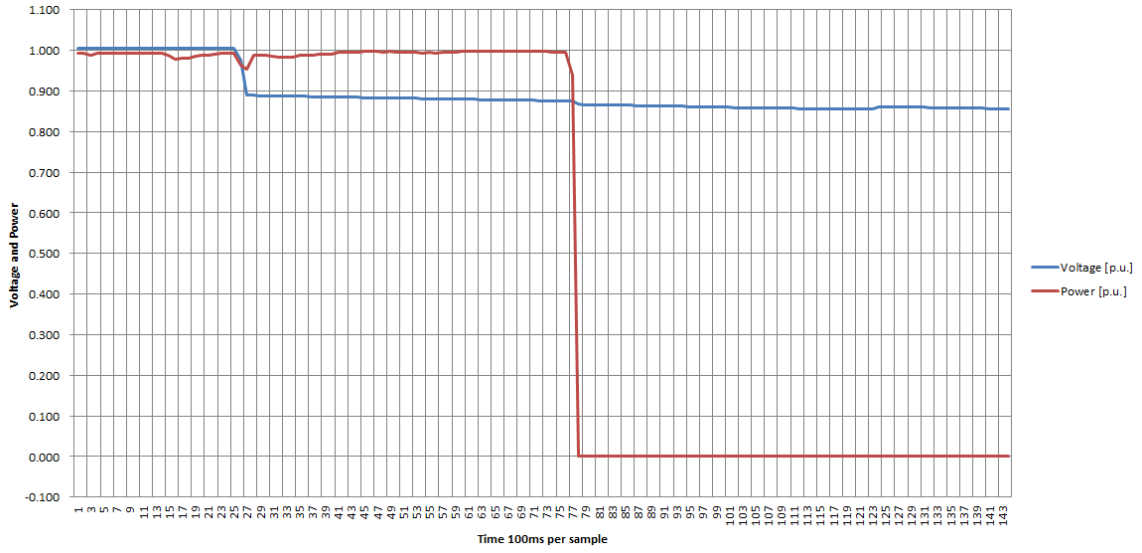
Under voltage, Stage 1 - Test 1

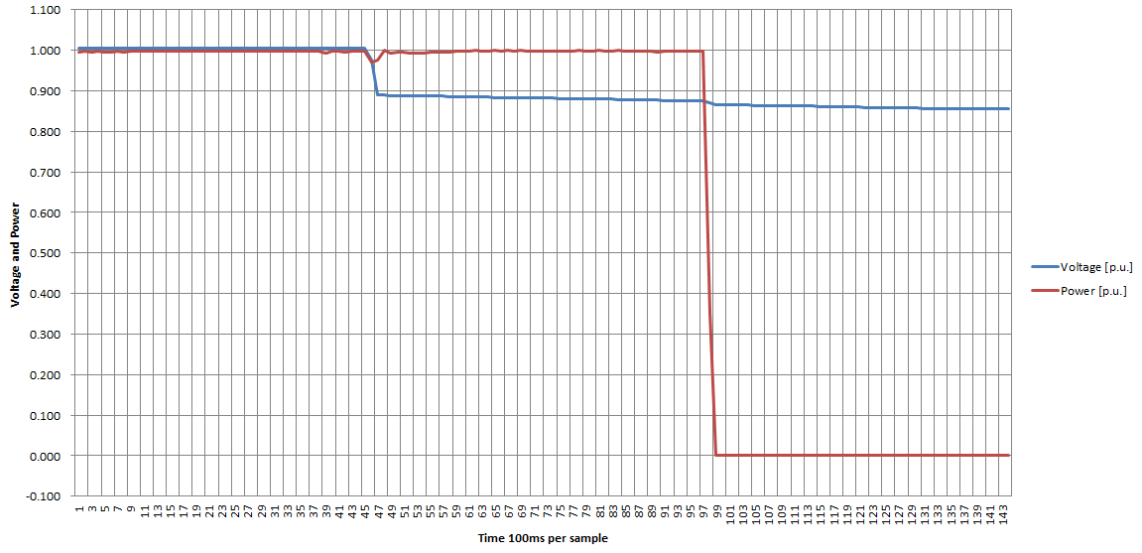


Under voltage, Stage 1 - Test 2



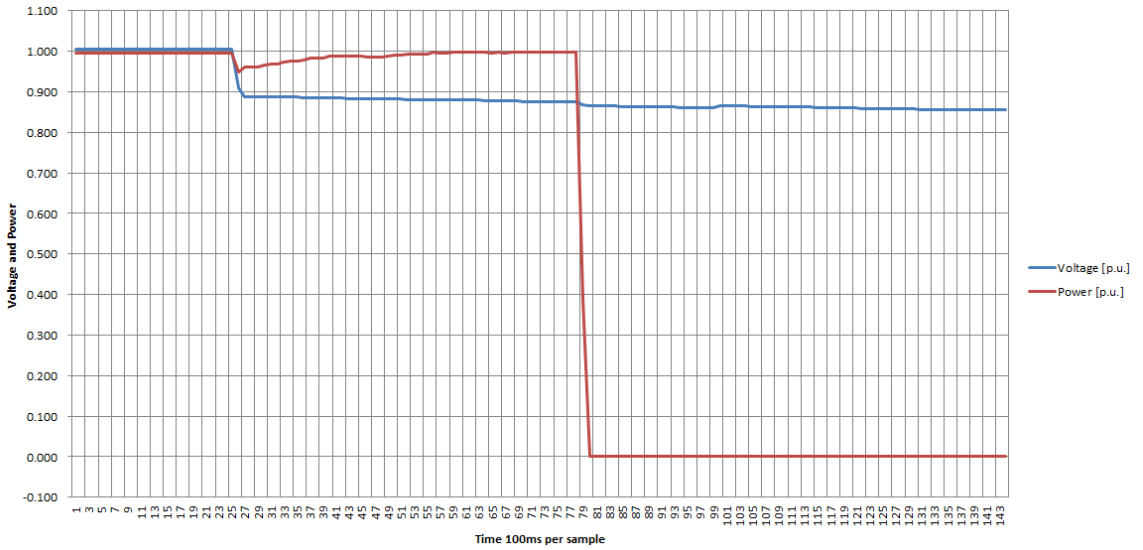
Appendix 1: Testing table

Under voltage, Stage 1 - Test 3


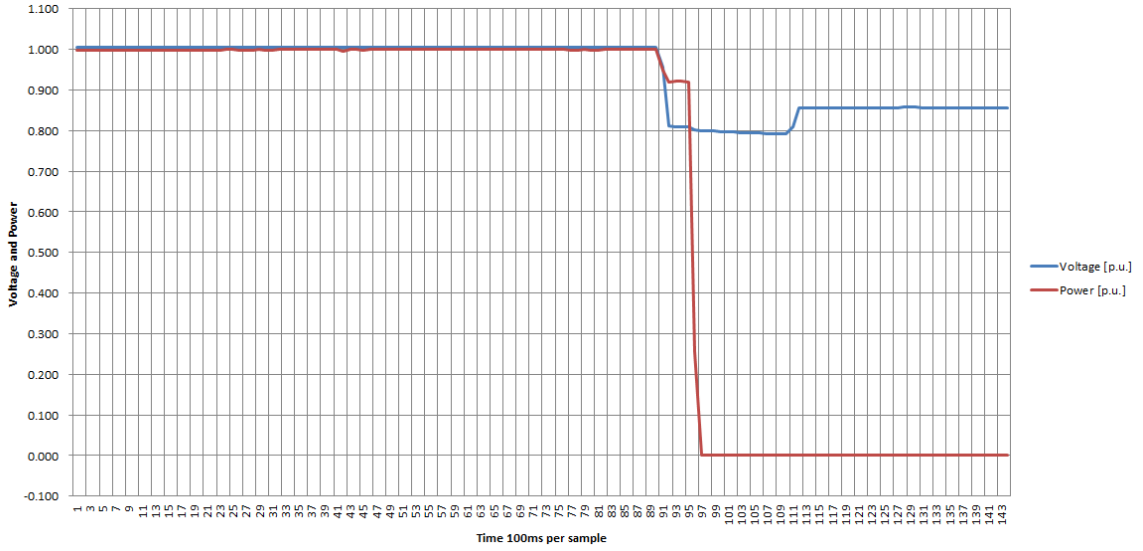
Under voltage, Stage 1 - Test 4


Appendix 1: Testing table

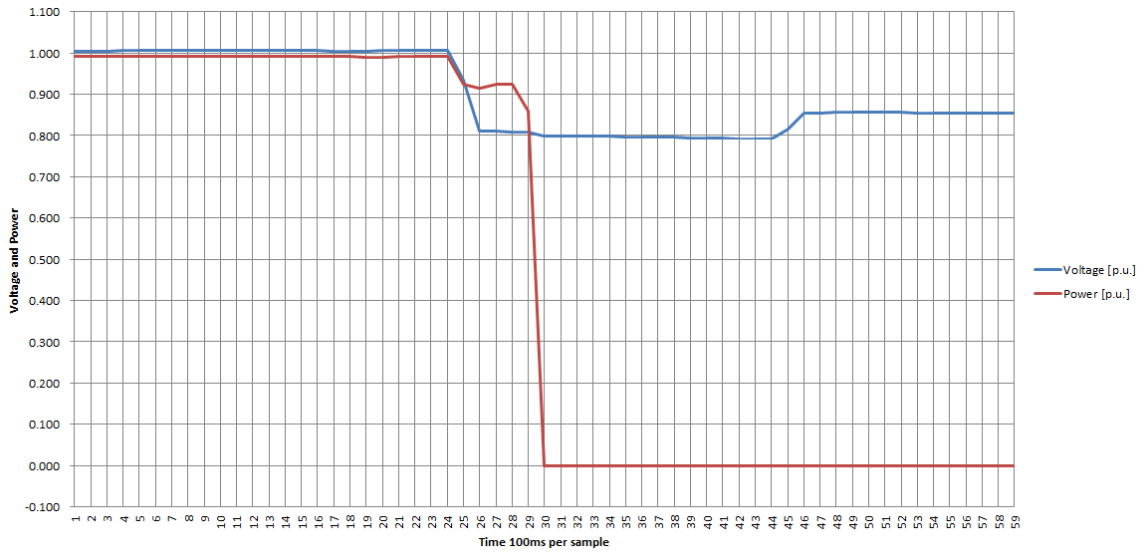
Under voltage, Stage 1 - Test 5

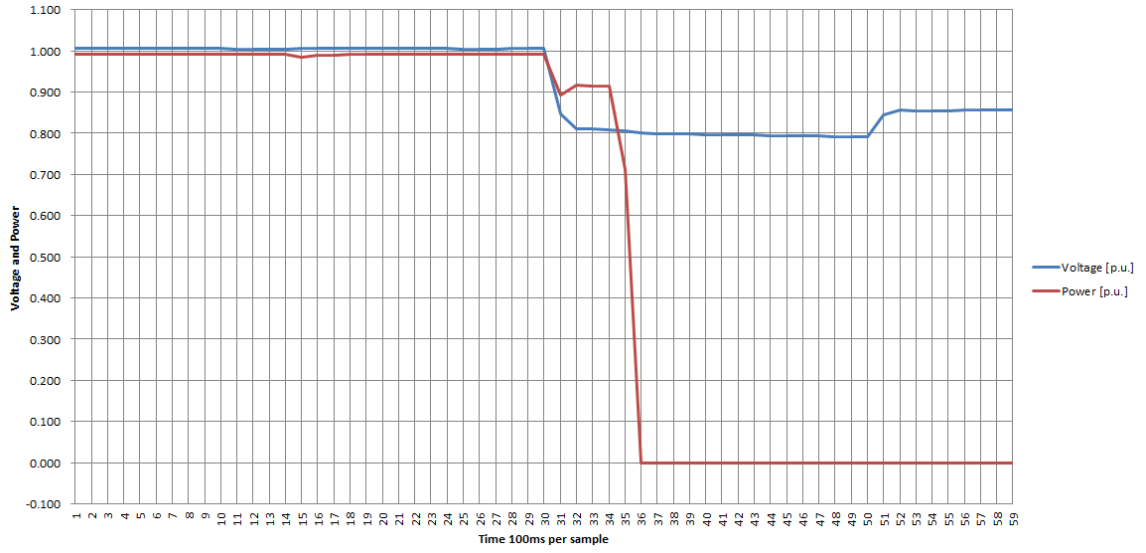


Under voltage, Stage 2 - Test 1



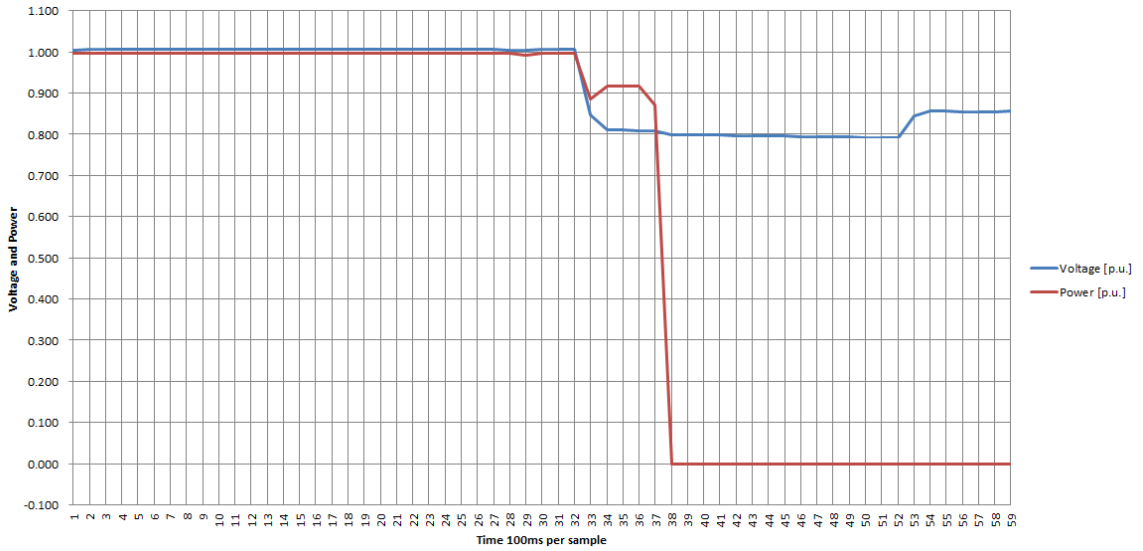
Appendix 1: Testing table

Under voltage, Stage 2 - Test 2


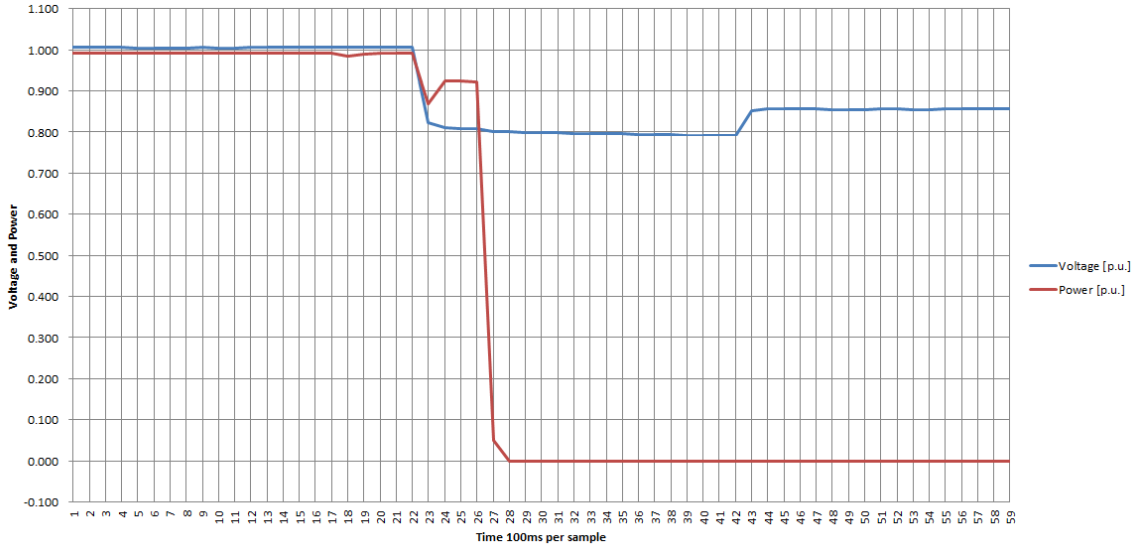
Under voltage, Stage 2 - Test 3


Appendix 1: Testing table

Under voltage, Stage 2 - Test 4

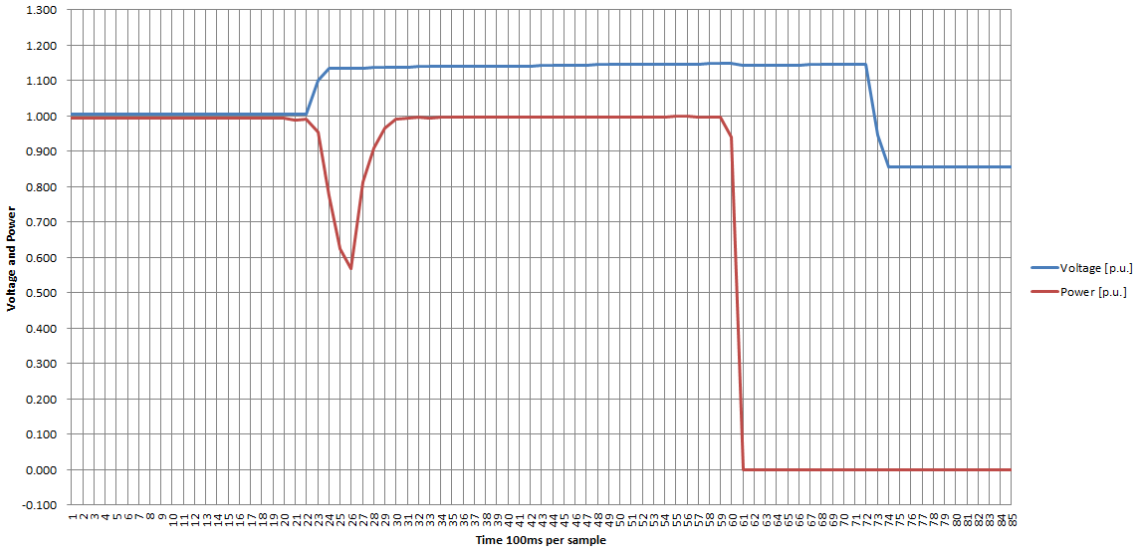


Under voltage, Stage 2 - Test 5

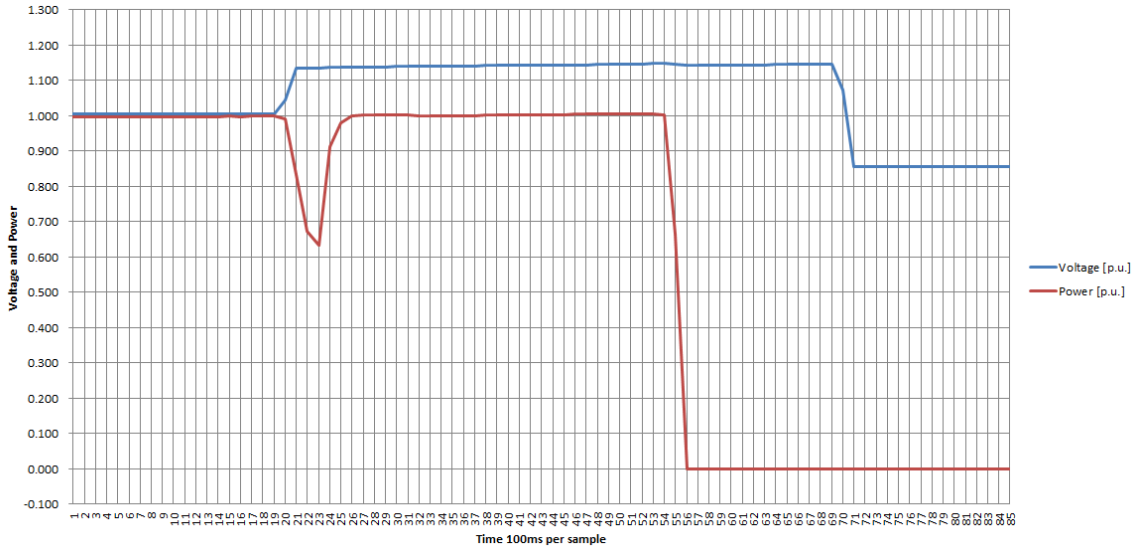


Appendix 1: Testing table

Over voltage, Stage 1 - Test 1

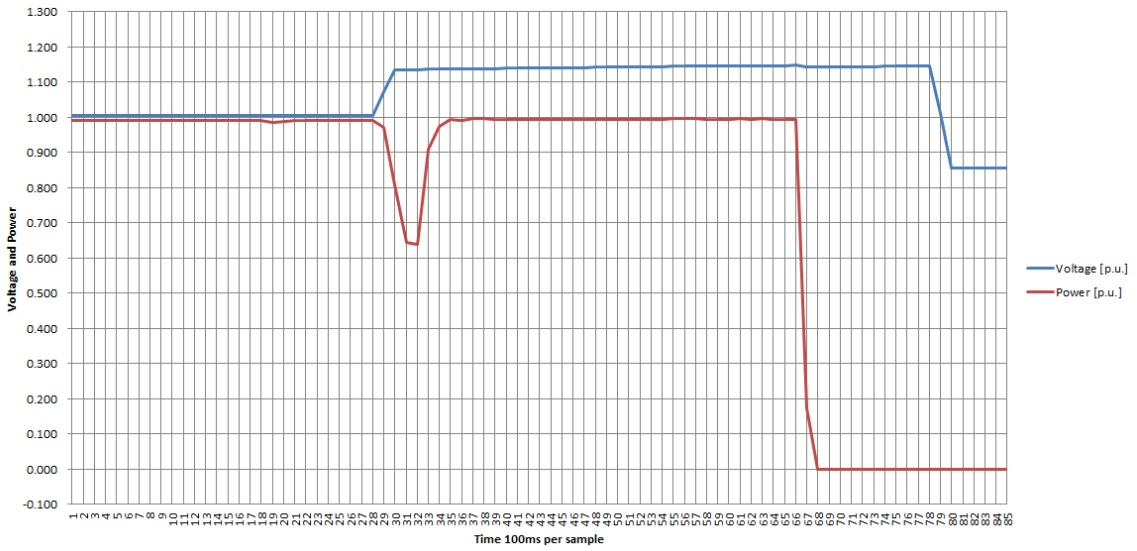


Over voltage, Stage 1 - Test 2

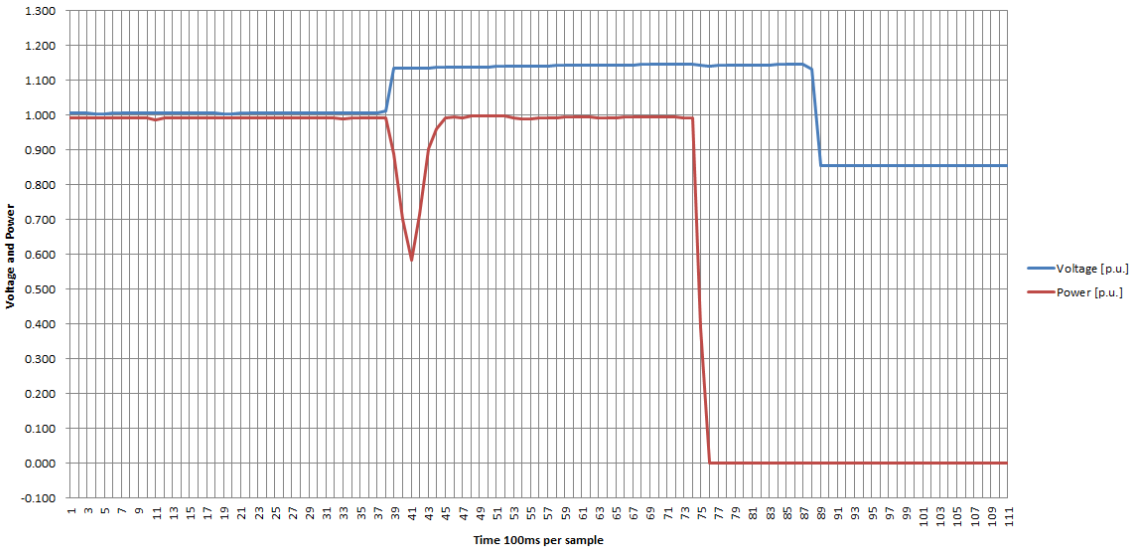


Appendix 1: Testing table

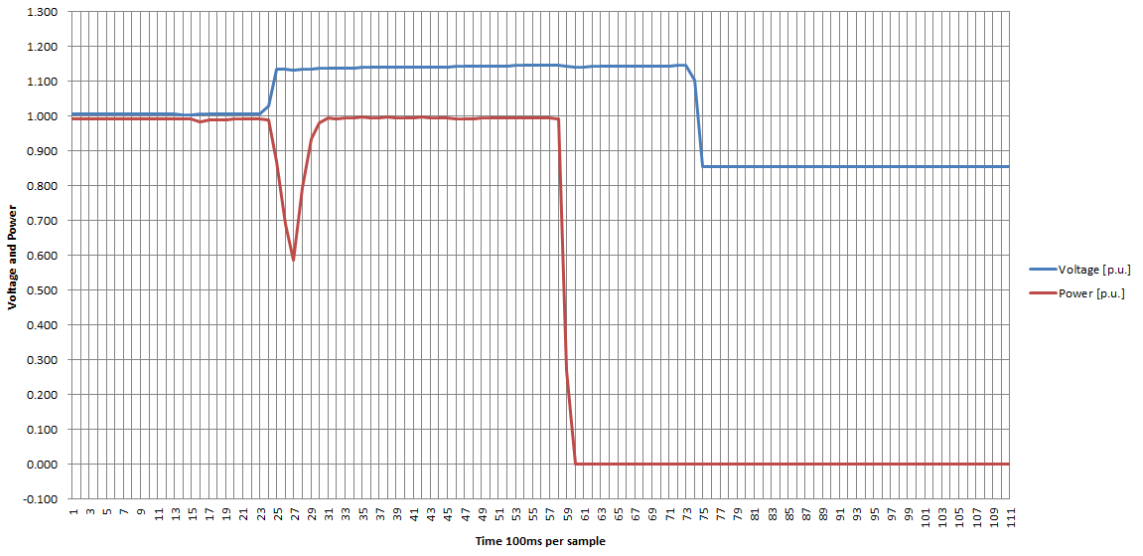
Over voltage, Stage 1 - Test 3

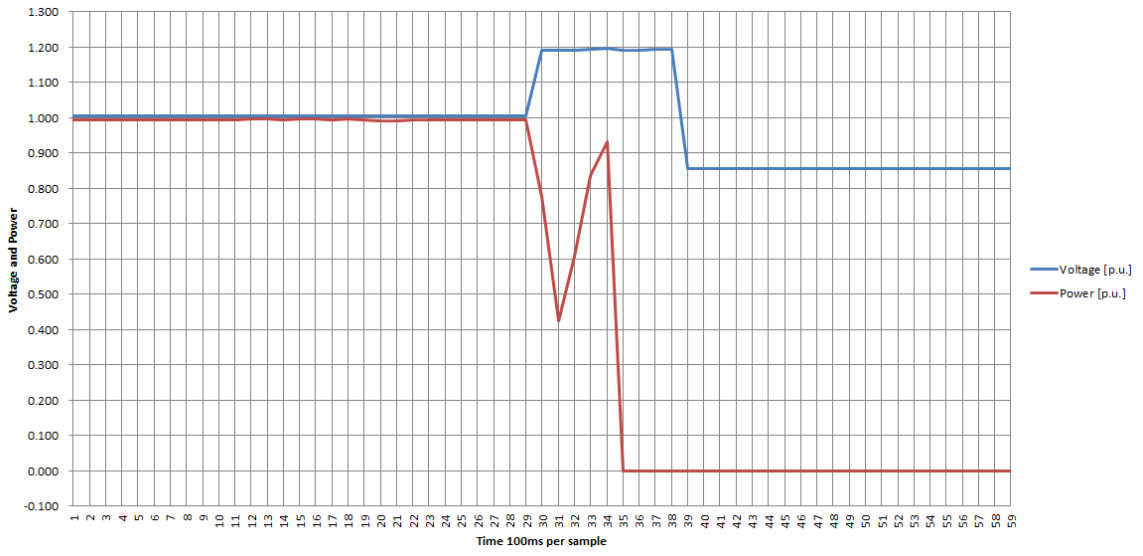


Over voltage, Stage 1 - Test 4



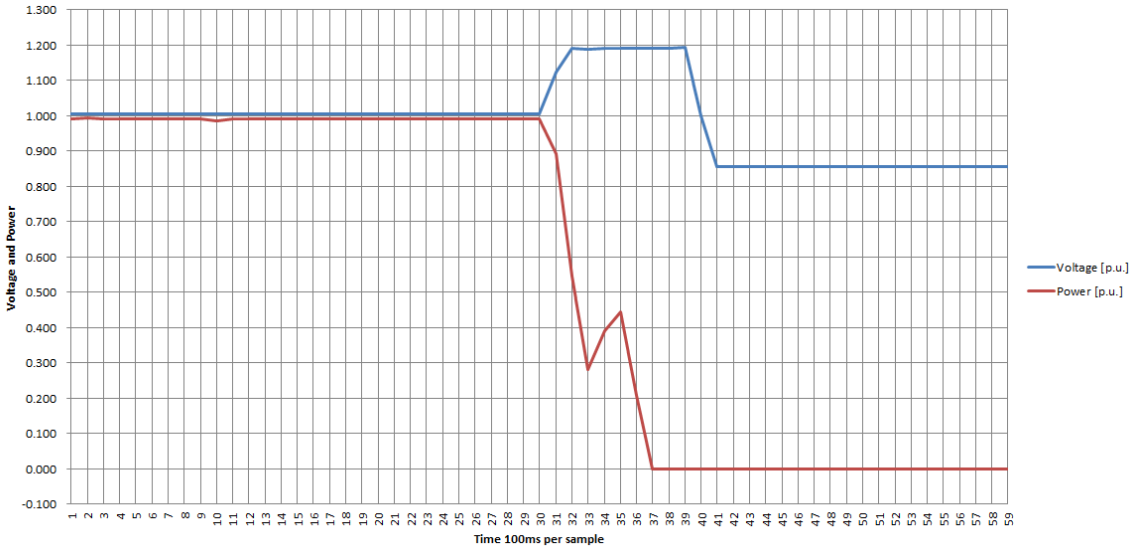
Appendix 1: Testing table

Over voltage, Stage 1 - Test 5


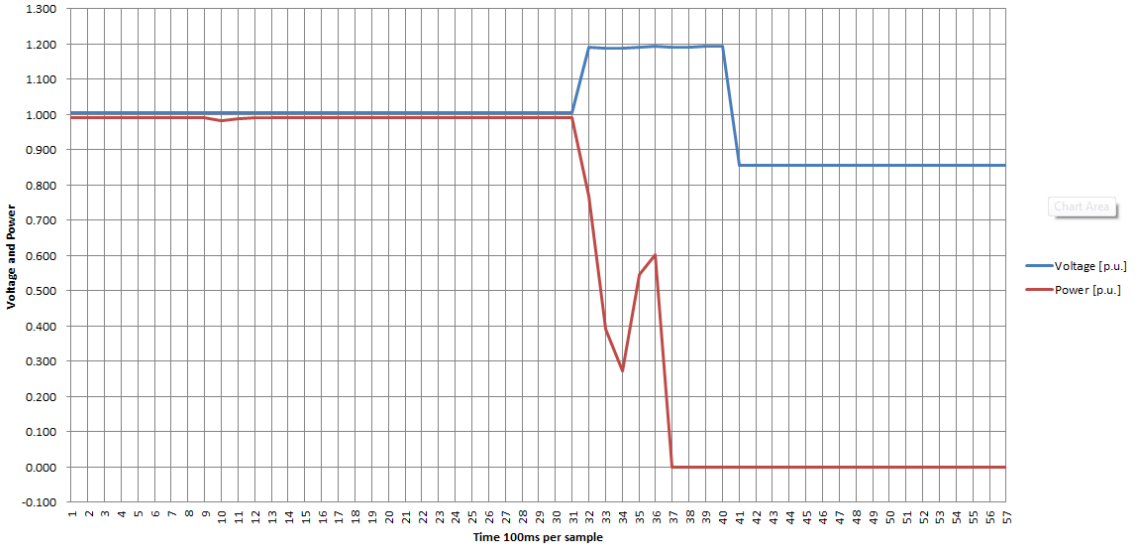
Over voltage, Stage 2 - Test 1


Appendix 1: Testing table

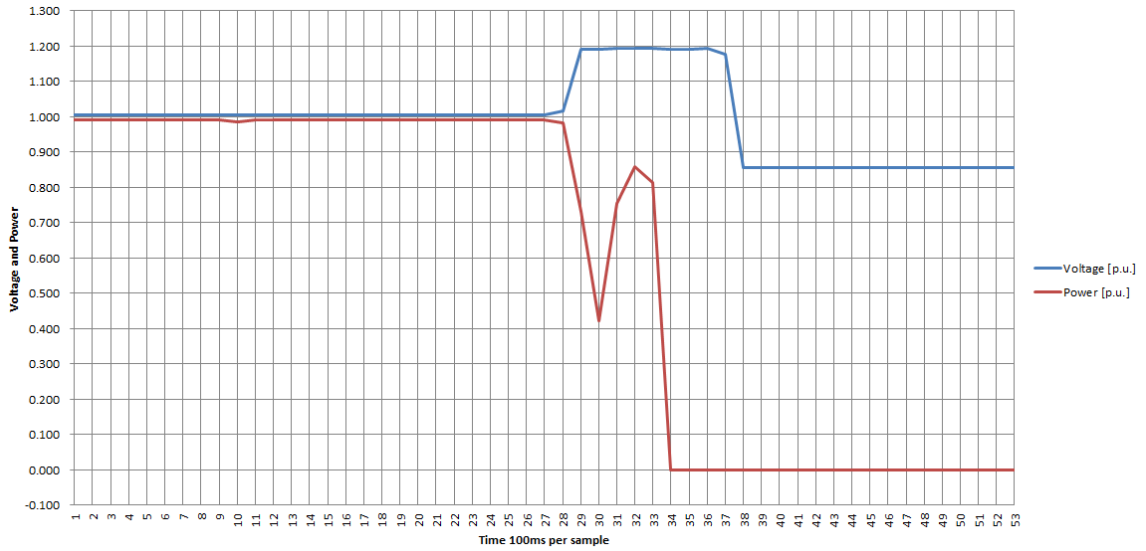
Over voltage, Stage 2 - Test 2

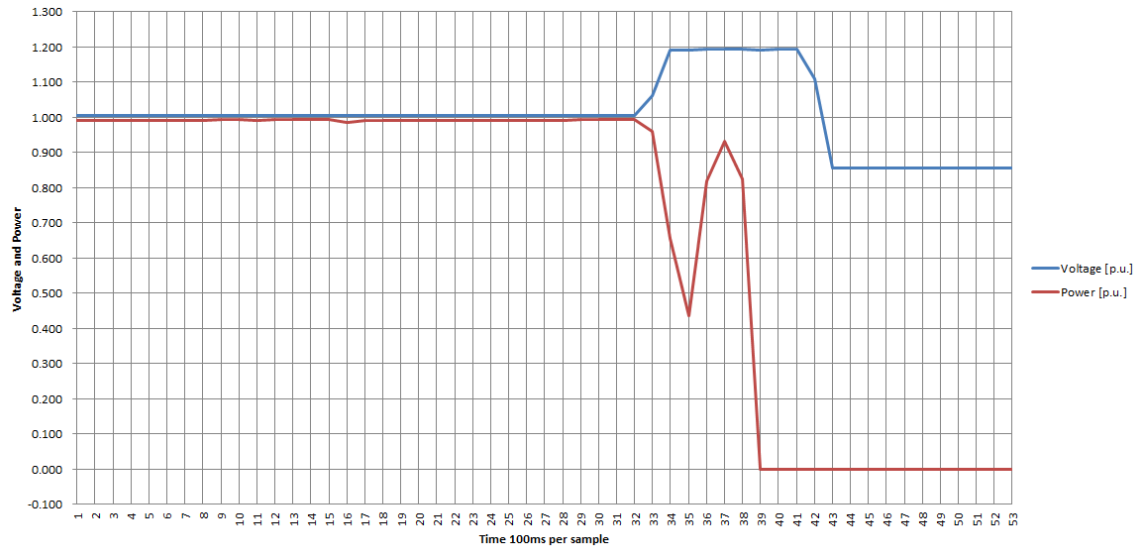


Over voltage, Stage 2 - Test 3



Appendix 1: Testing table

Over voltage, Stage 2 - Test 4


Over voltage, Stage 2 - Test 5


Appendix 1: Testing table

Trip time test.

The tests have been made as the following procedure:

- For undervoltage protection: Starting from a voltage level 2%Un above the trip value of the protection function to be tested, the voltage is decreased in a step of 4%Un and it is measured from that instant the time it takes to disconnect.
- For overvoltage protection: Starting from a voltage level 2%Un below the trip value of the protection function to be tested, the voltage is increased in a step of 4%Un and it is measured from that instant the time it takes to disconnect.

Trips have been repeated 5 times at each voltage level.

Following tables show the test results:

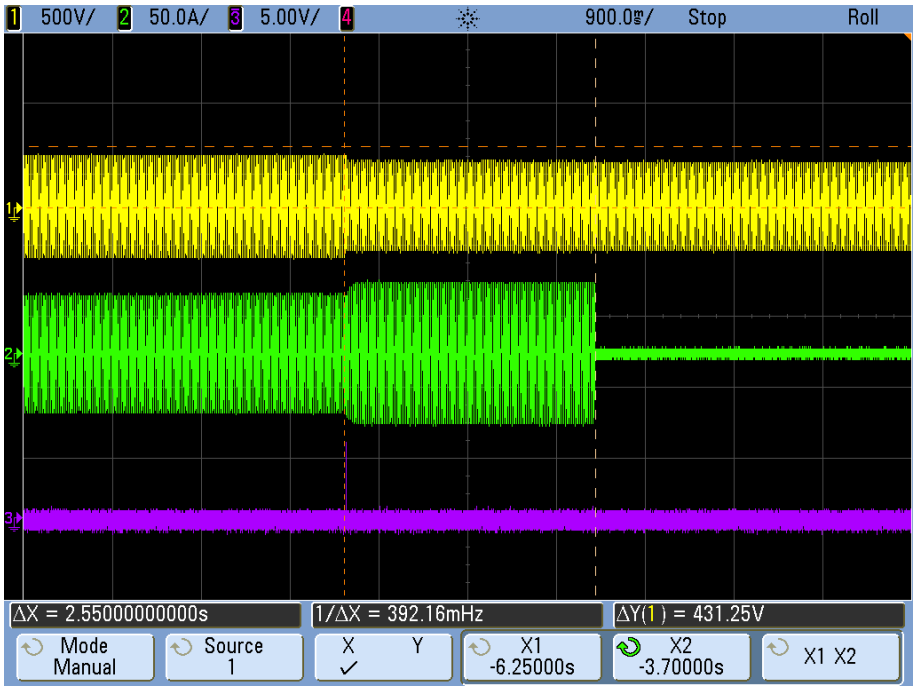
Appendix 1: Testing table

Stage/Prot Function	Test	Delay Time limit (s)	Maximum trip time (s)	Trip time measured (s)	Disconnection
U/V st1 87% Un	1	2.5	3.0	2.550	☐ NO ☒ YES
	2	2.5	3.0	2.547	☐ NO ☒ YES
	3	2.5	3.0	2.556	☐ NO ☒ YES
	4	2.5	3.0	2.547	☐ NO ☒ YES
	5	2.5	3.0	2.556	☐ NO ☒ YES
U/V st2 80% Un	1	0.5	1.0	0.528	☐ NO ☒ YES
	2	0.5	1.0	0.520	☐ NO ☒ YES
	3	0.5	1.0	0.518	☐ NO ☒ YES
	4	0.5	1.0	0.528	☐ NO ☒ YES
	5	0.5	1.0	0.520	☐ NO ☒ YES
O/V st1 114% Un	1	1.0	1.5	1.030	☐ NO ☒ YES
	2	1.0	1.5	1.035	☐ NO ☒ YES
	3	1.0	1.5	1.050	☐ NO ☒ YES
	4	1.0	1.5	1.040	☐ NO ☒ YES
	5	1.0	1.5	1.050	☐ NO ☒ YES
O/V st2 119% Un	1	0.5	1.0	0.520	☐ NO ☒ YES
	2	0.5	1.0	0.530	☐ NO ☒ YES
	3	0.5	1.0	0.532	☐ NO ☒ YES
	4	0.5	1.0	0.528	☐ NO ☒ YES
	5	0.5	1.0	0.520	☐ NO ☒ YES

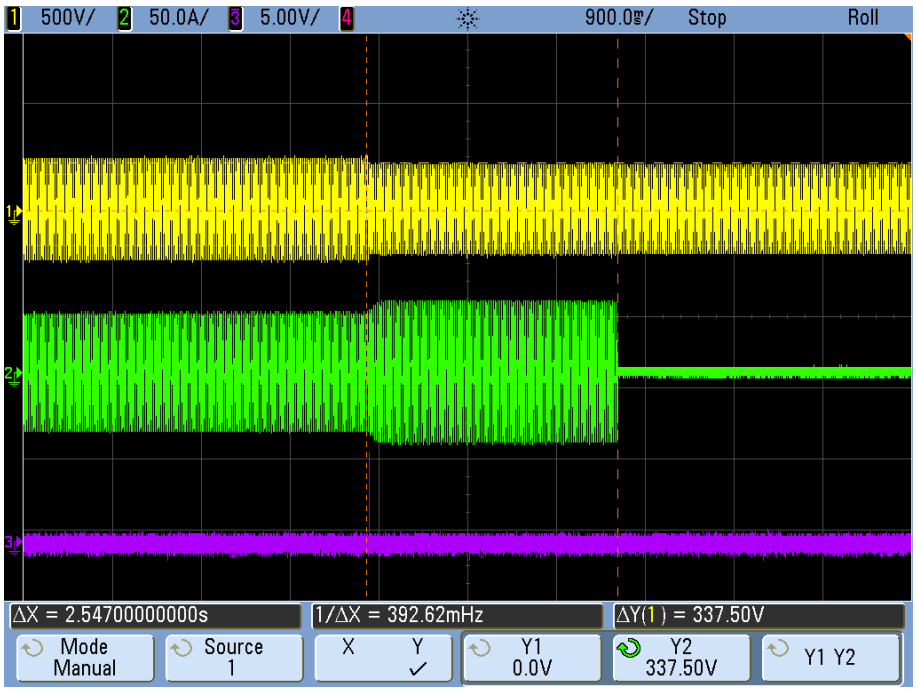
Test results are graphically shown in following pages.

Appendix 1: Testing table

Under voltage, Stage 1 - Test 1

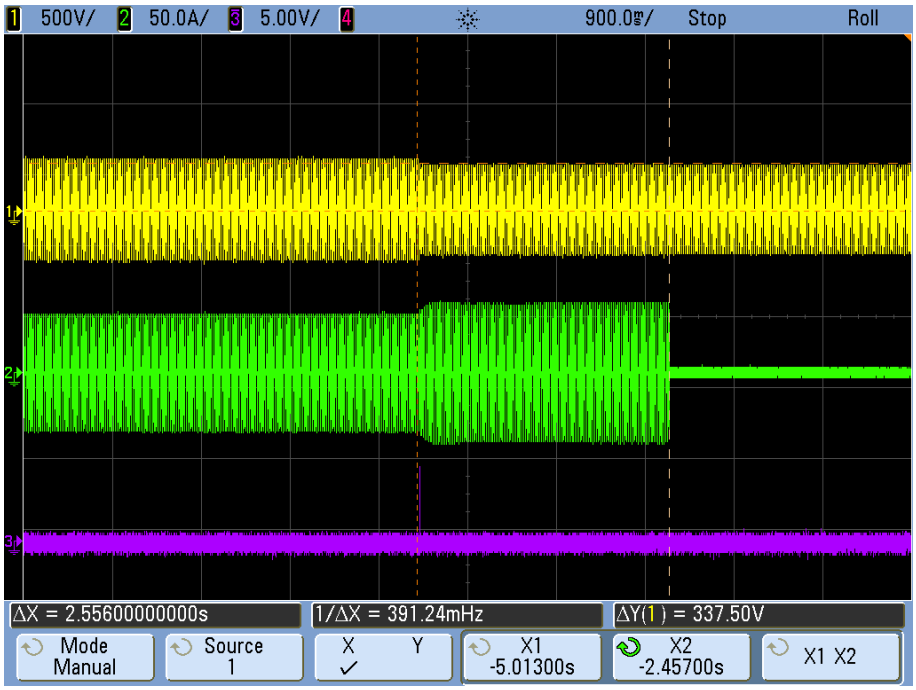


Under voltage, Stage 1 - Test 2

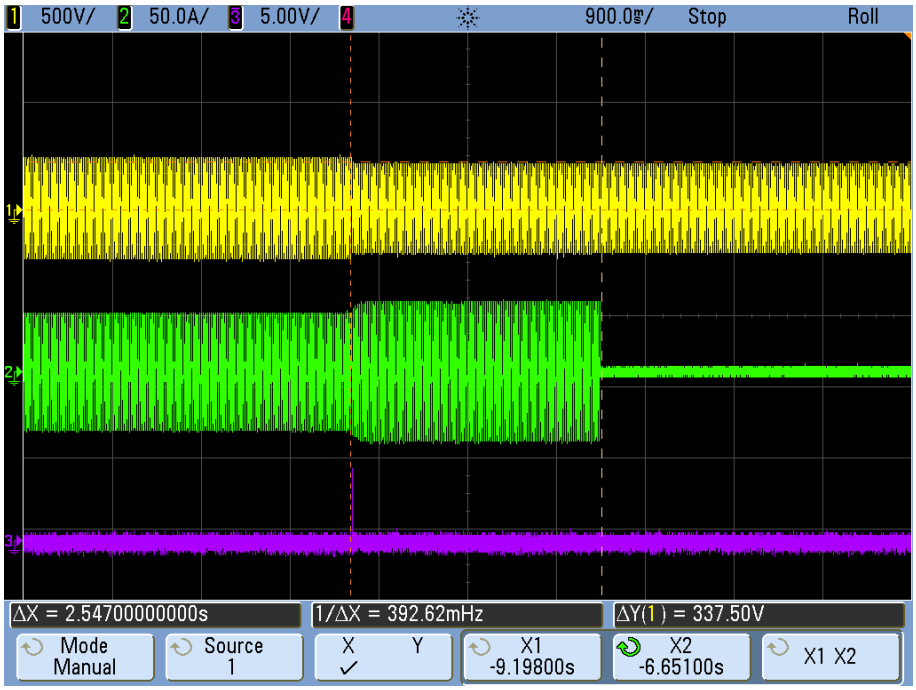


Appendix 1: Testing table

Under voltage, Stage 1 - Test 3



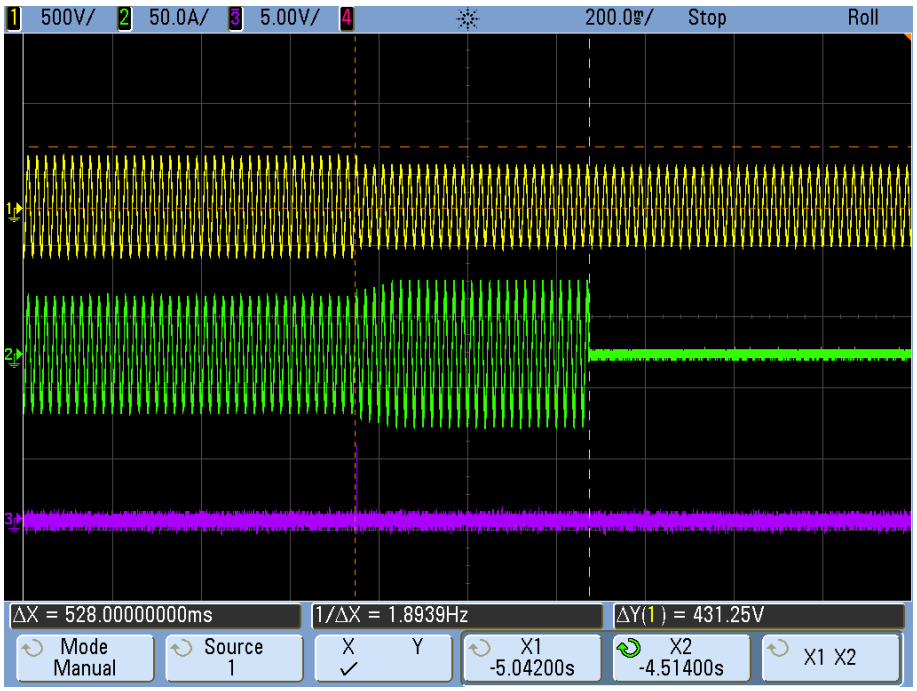
Under voltage, Stage 1 - Test 4



Appendix 1: Testing table

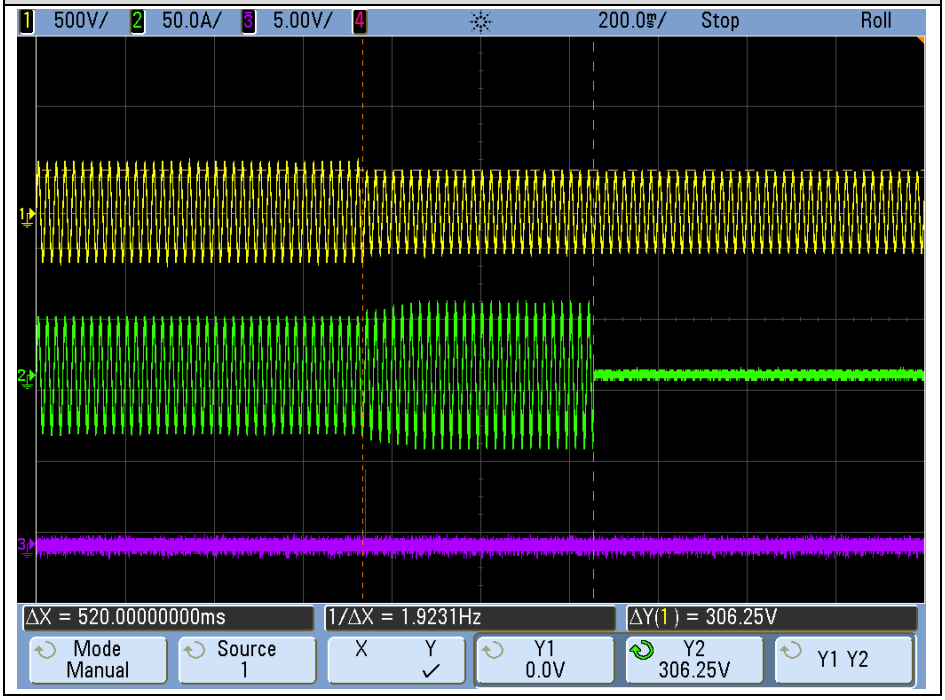
Under voltage, Stage 1 - Test 5

Under voltage, Stage 2 - Test 1

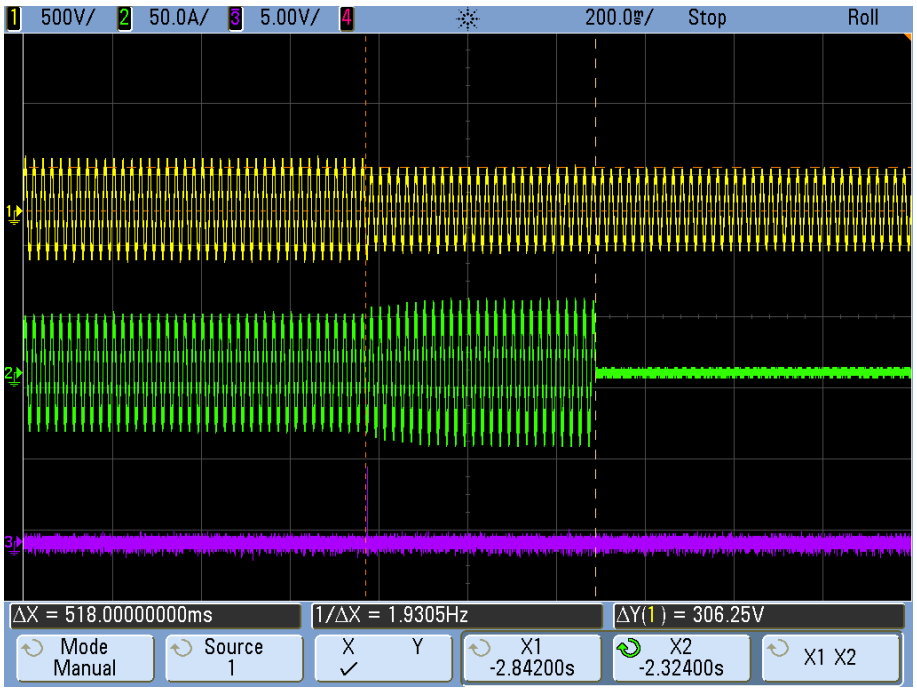


Appendix 1: Testing table

Under voltage, Stage 2 - Test 2

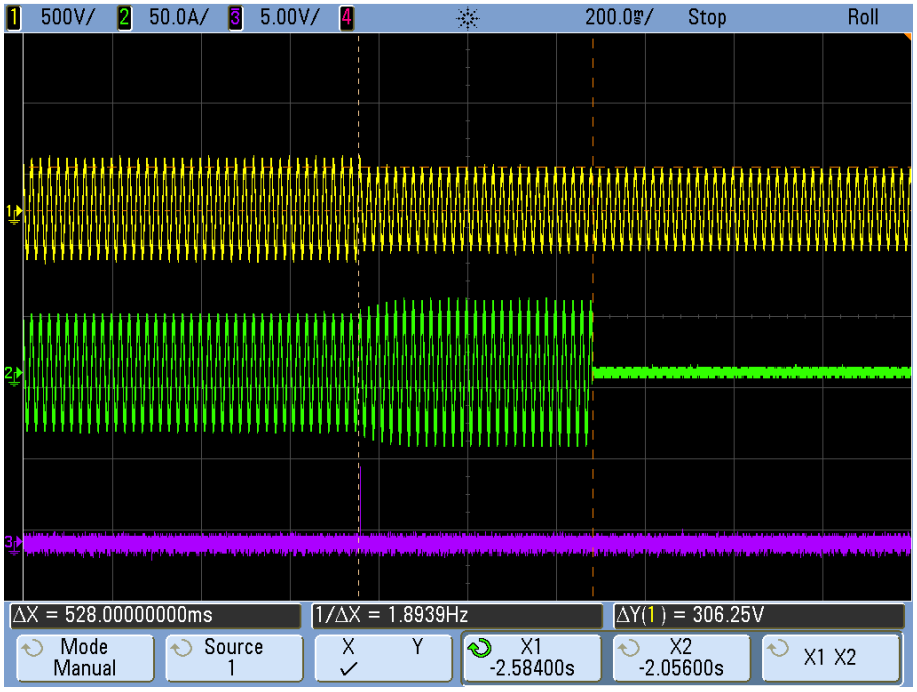


Under voltage, Stage 2 - Test 3

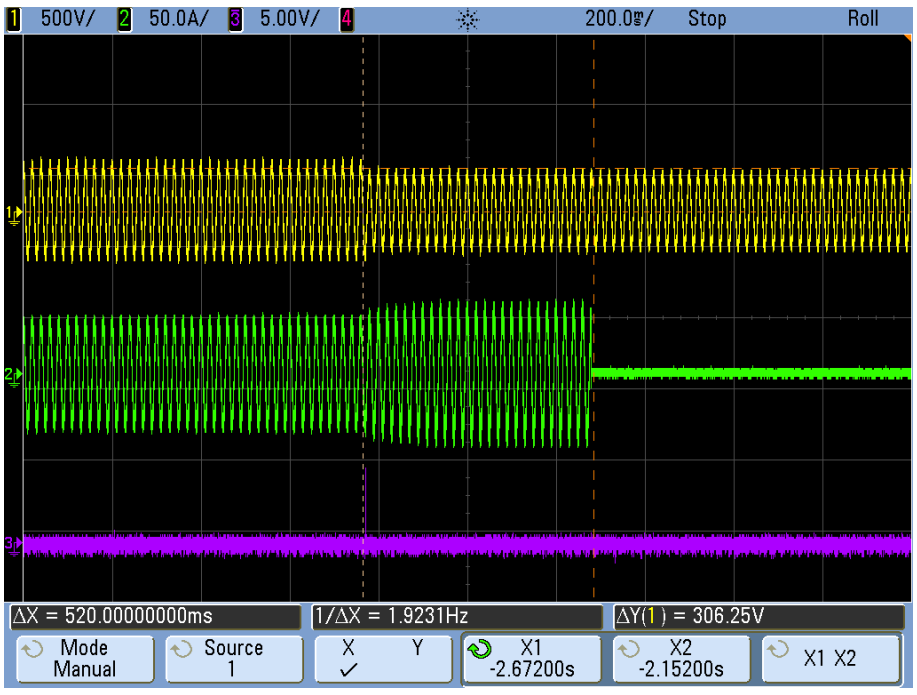


Appendix 1: Testing table

Under voltage, Stage 2 - Test 4

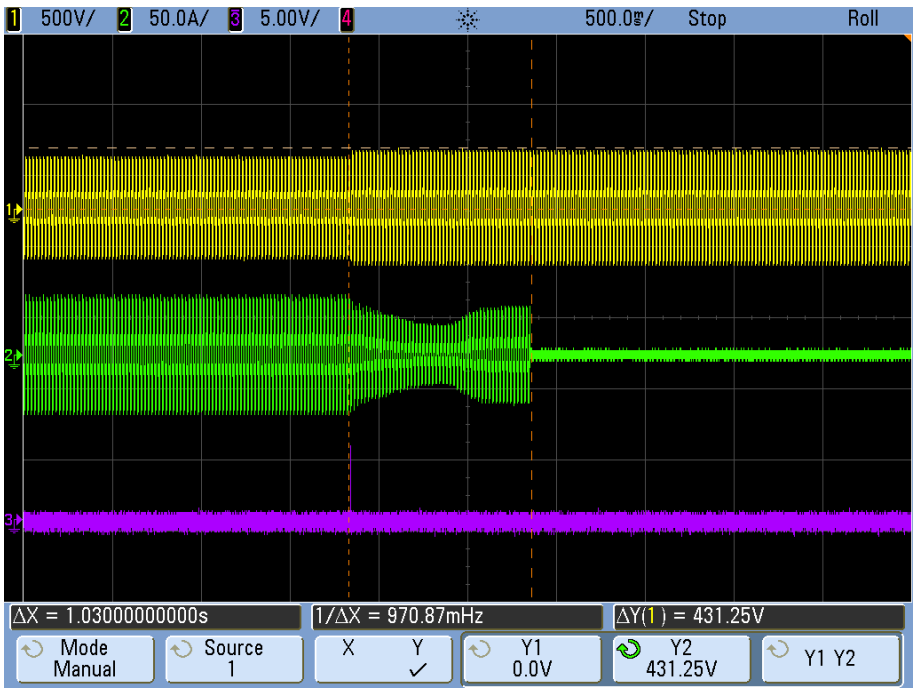


Under voltage, Stage 2 - Test 5

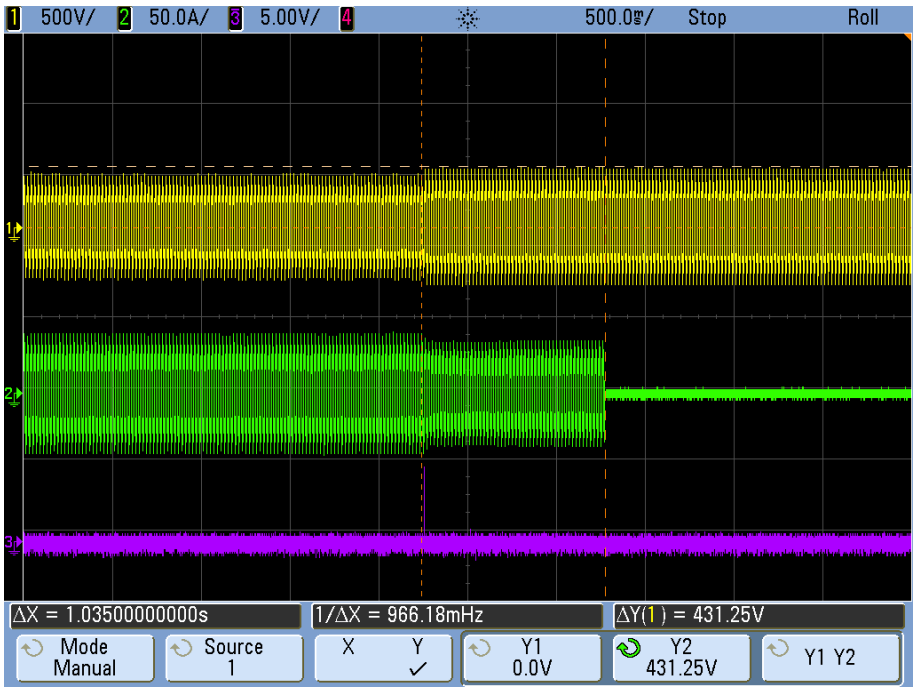


Appendix 1: Testing table

Over voltage, Stage 1 - Test 1

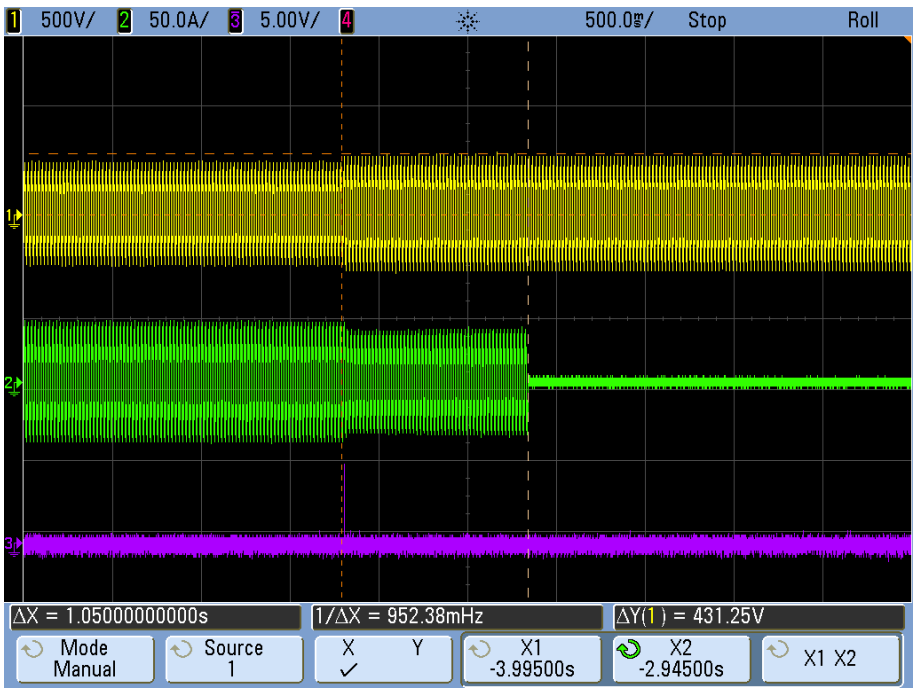


Over voltage, Stage 1 - Test 2

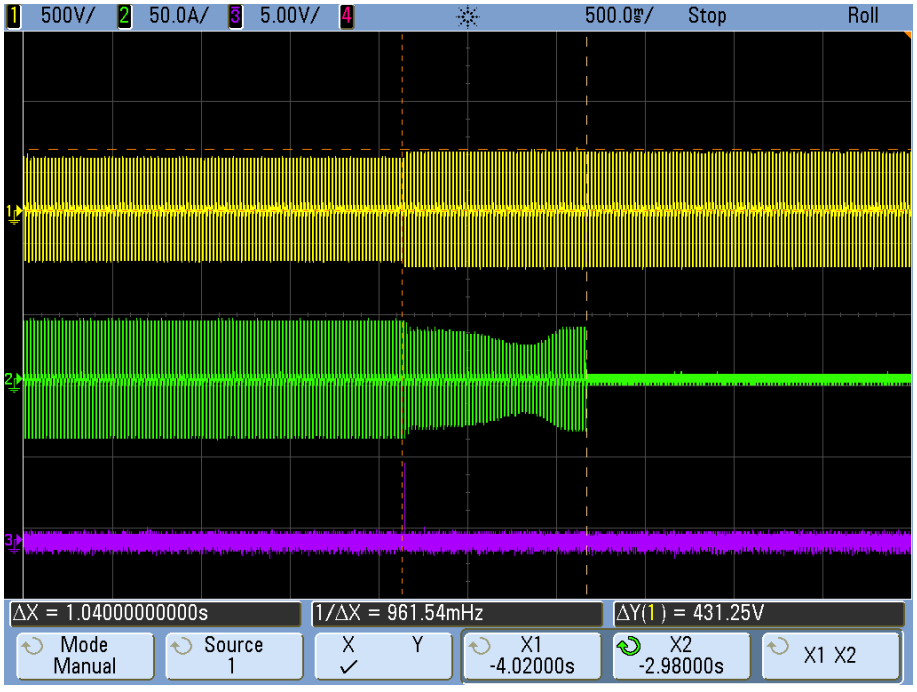


Appendix 1: Testing table

Over voltage, Stage 1 - Test 3

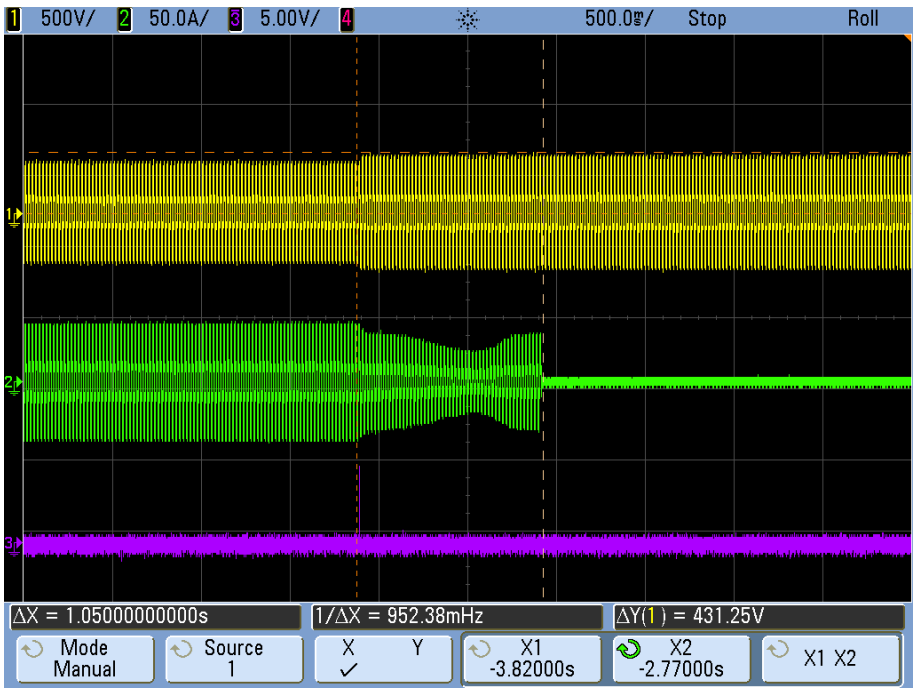


Over voltage, Stage 1 - Test 4

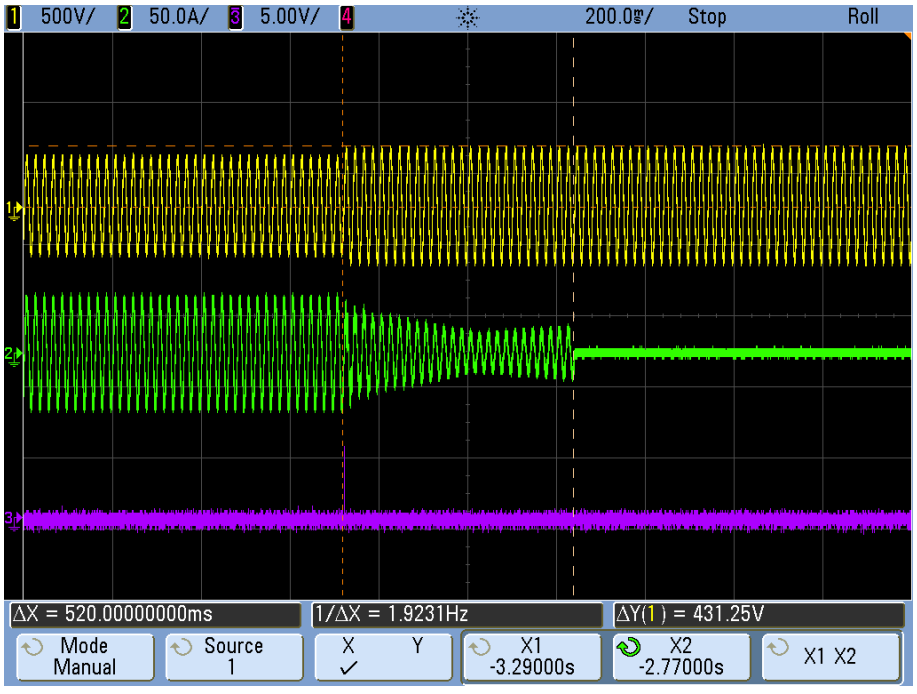


Appendix 1: Testing table

Over voltage, Stage 1 - Test 5

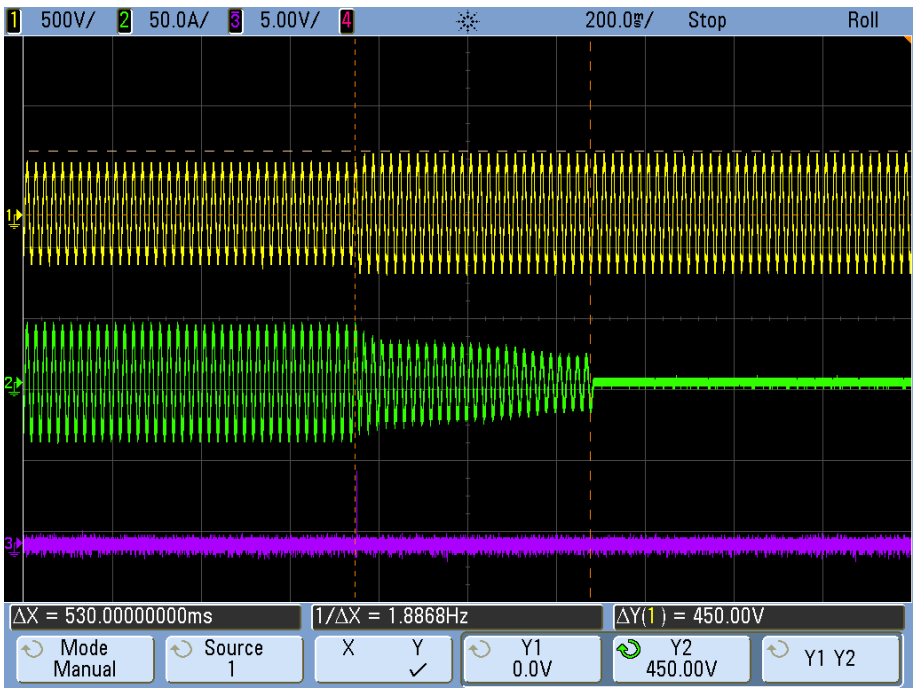


Over voltage, Stage 2 - Test 1

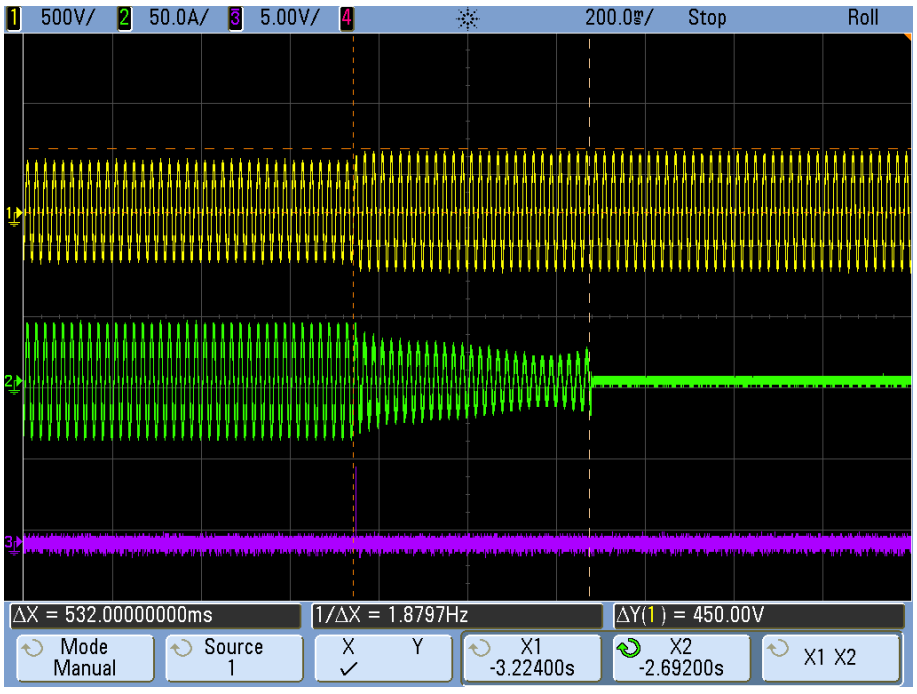


Appendix 1: Testing table

Over voltage, Stage 2 - Test 2

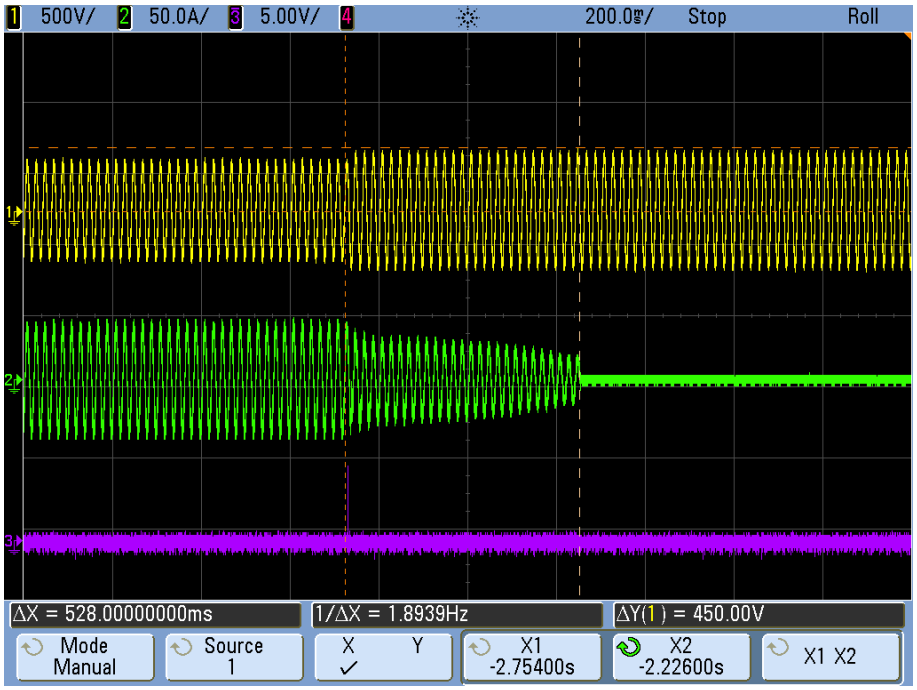


Over voltage, Stage 2 - Test 3



Appendix 1: Testing table

Over voltage, Stage 2 - Test 4



Over voltage, Stage 2 - Test 5

Appendix 1: Testing table

No trip Tests

To ensure that the protection will not trip in error voltage and frequency, “no-trip tests” have been carried out at frequencies, voltages and time configurations detailed bellow.

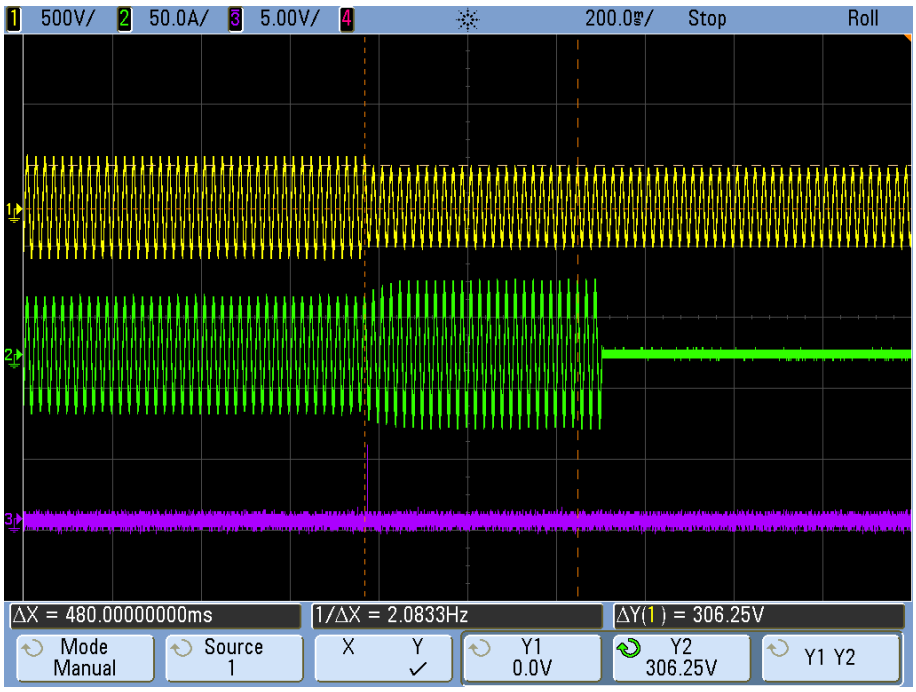
The test procedure consists in leading the inverter out from its normal conditions with a step to the set-point of frequency or voltage established at the tables below and maintain the step for the time desired, once reached the time desired the inverter is taken back to the normal conditions, the inverter shall not trip during the test.

Voltage no-trip tests

Test No	Voltage setting (V)	Time required (s)	Time measured (s)	Disconnection
1	180.0	0.48	0.48	☒ NO ☐ YES
2	188.0	2.48	2.48	☒ NO ☐ YES
3	204.1	3.5	3.5	☒ NO ☐ YES
4	258.2	2.0	2.0	☒ NO ☐ YES
5	269.7	0.98	0.98	☒ NO ☐ YES
6	277.7	0.48	0.48	☒ NO ☐ YES

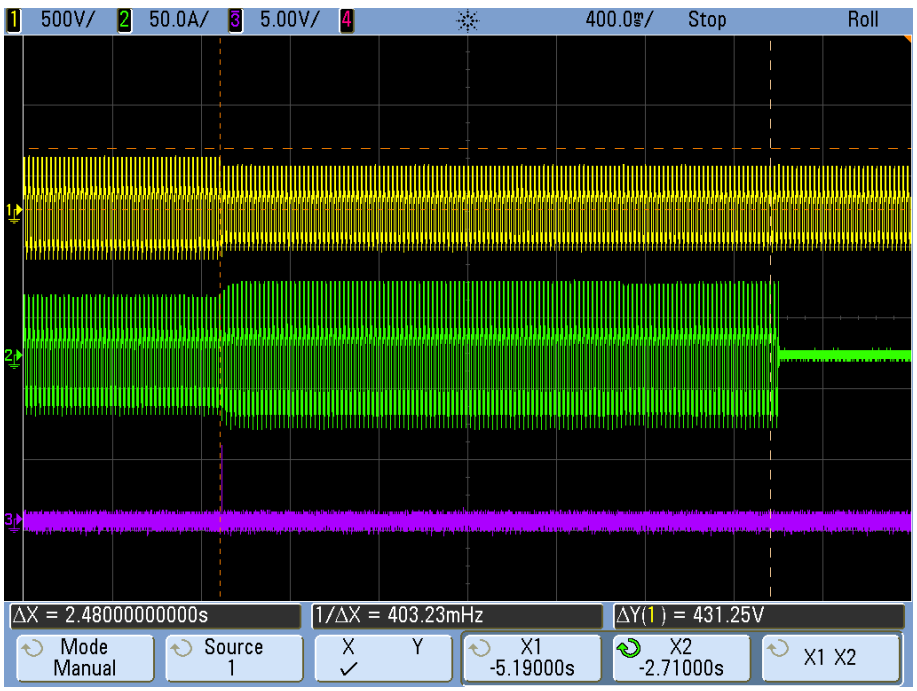
Test results are graphically shown in following pages.

Voltage no-trip tests - Test 1

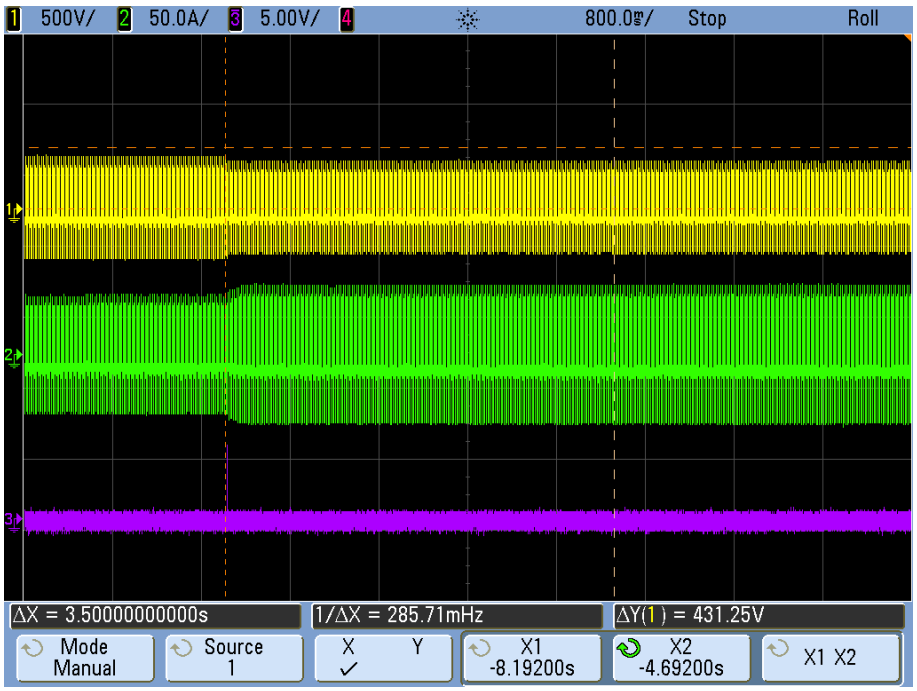


Appendix 1: Testing table

Voltage no-trip tests - Test 2

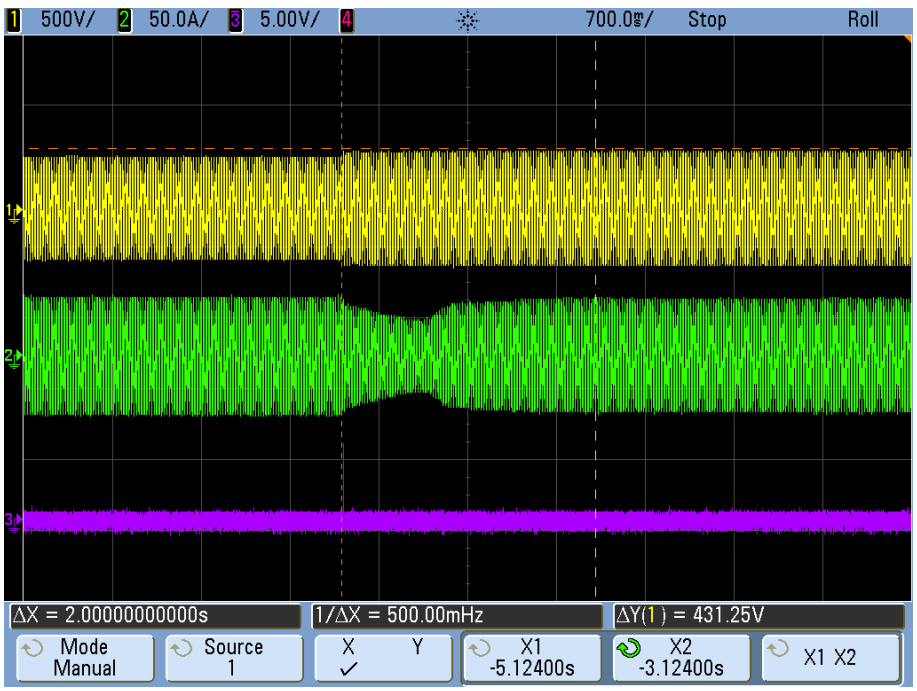


Voltage no-trip tests - Test 3

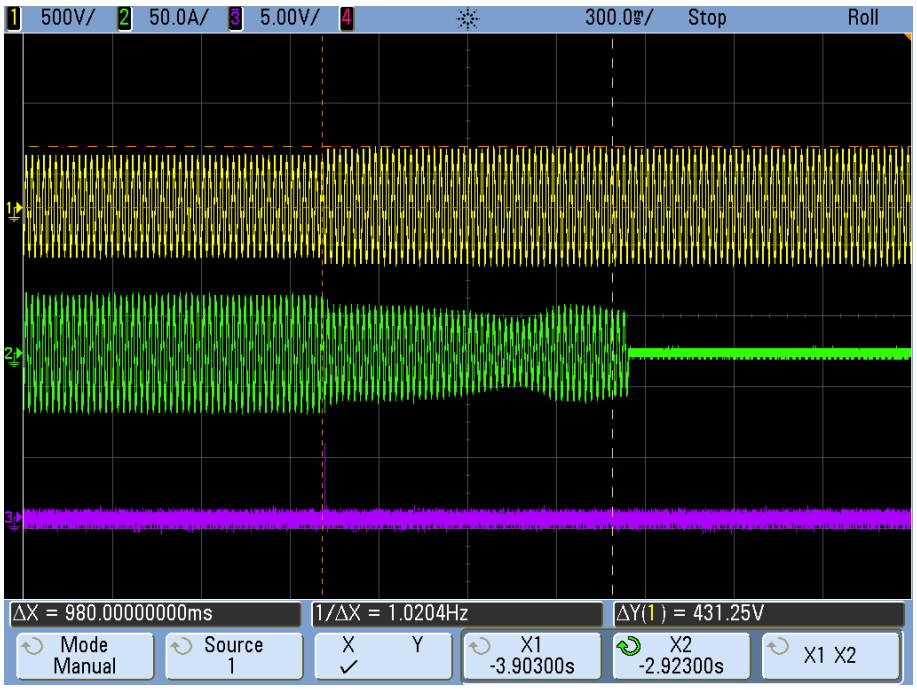


Appendix 1: Testing table

Voltage no-trip tests - Test 4

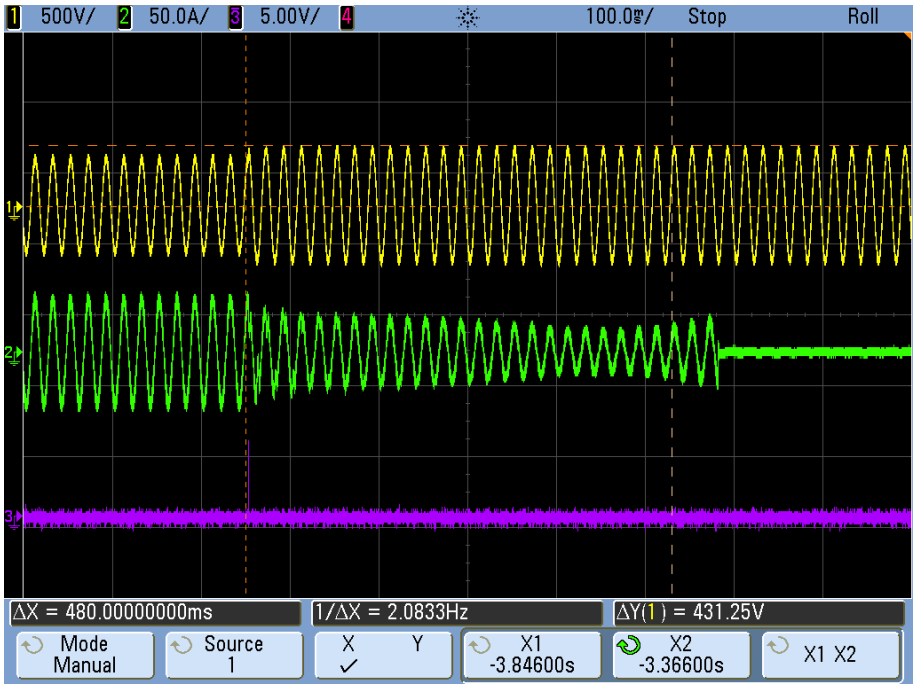


Voltage no-trip tests - Test 5



Appendix 1: Testing table

Voltage no-trip tests - Test 6



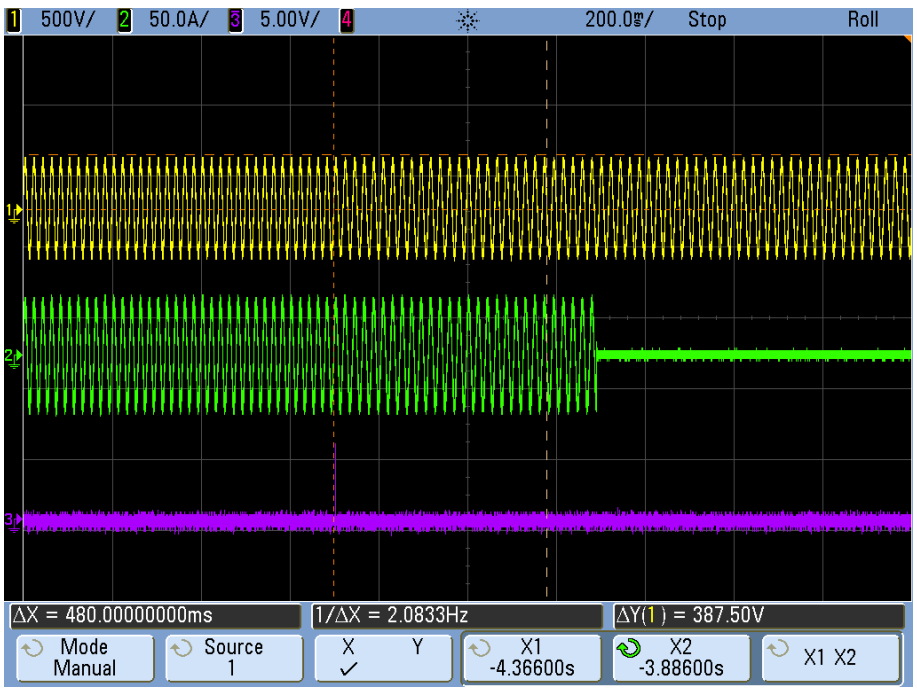
Frequency no-trip tests

Test No.	Frequency setting (Hz)	Time required (s)	Time measured (s)	Disconnection
1	46.8	0.48	0.48	☒ NO ☐ YES
2	47.2	19.98	19.98	☒ NO ☐ YES
3	47.7	25	25	☒ NO ☐ YES
4	51.3	95	95	☒ NO ☐ YES
5	51.8	89.98	89.98	☒ NO ☐ YES
6	52.5	0.48	0.48	☒ NO ☐ YES

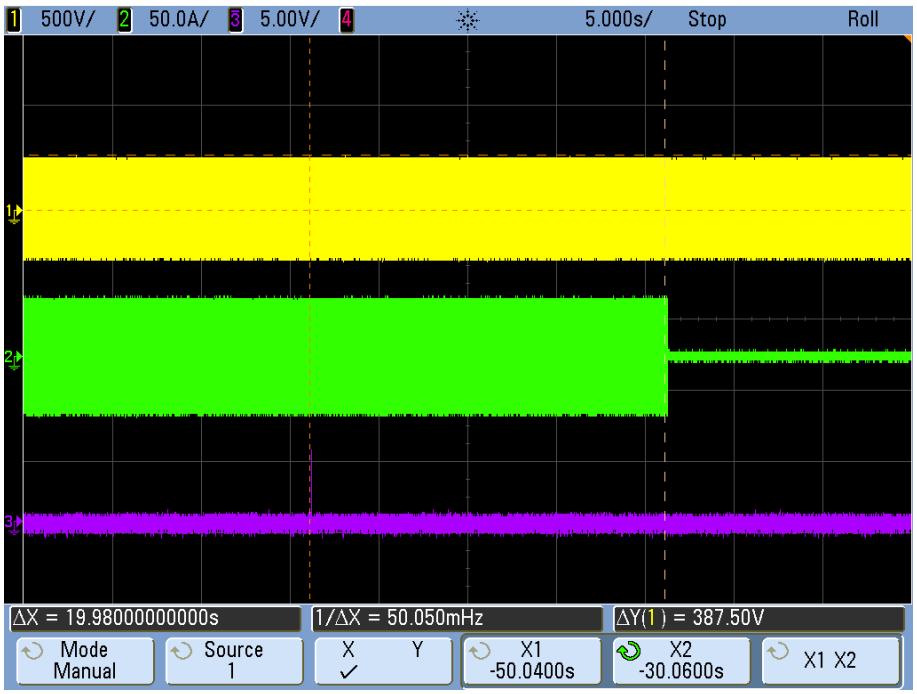
Test results are graphically shown in following pages.

Appendix 1: Testing table

Frequency no-trip tests - Test 1

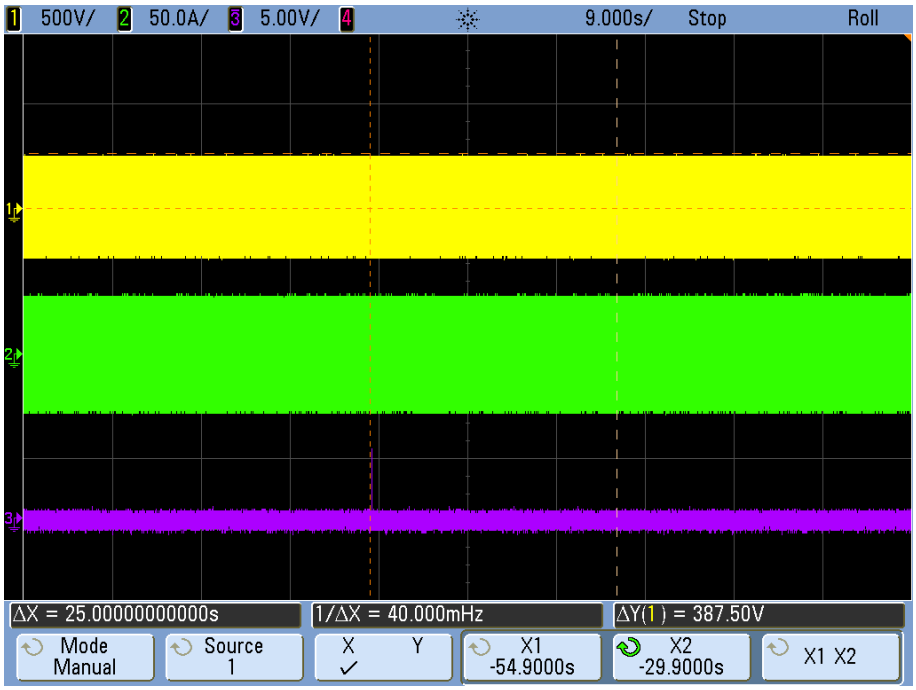


Frequency no-trip tests - Test 2

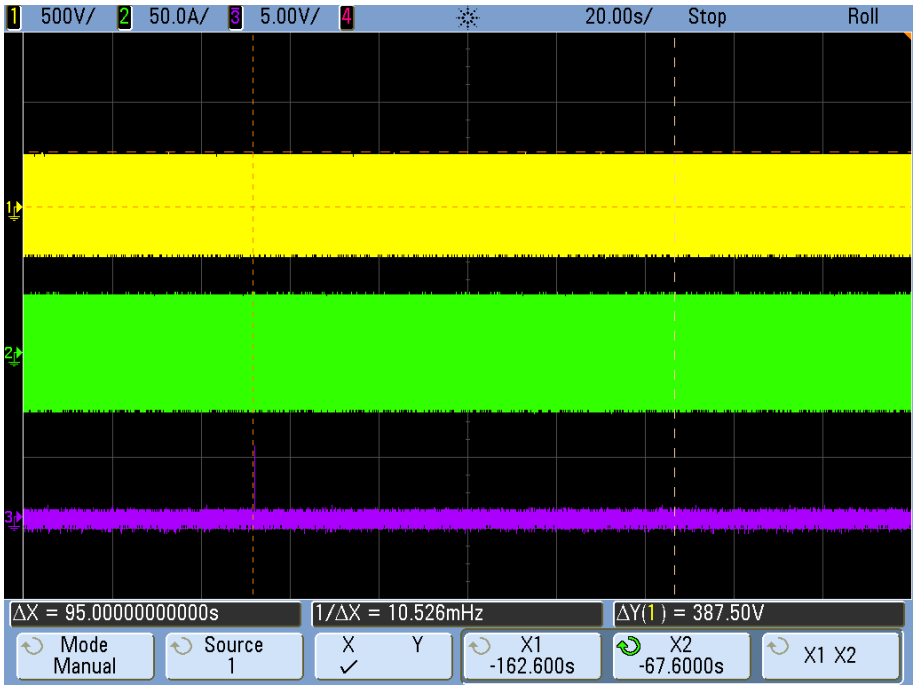


Appendix 1: Testing table

Frequency no-trip tests - Test 3



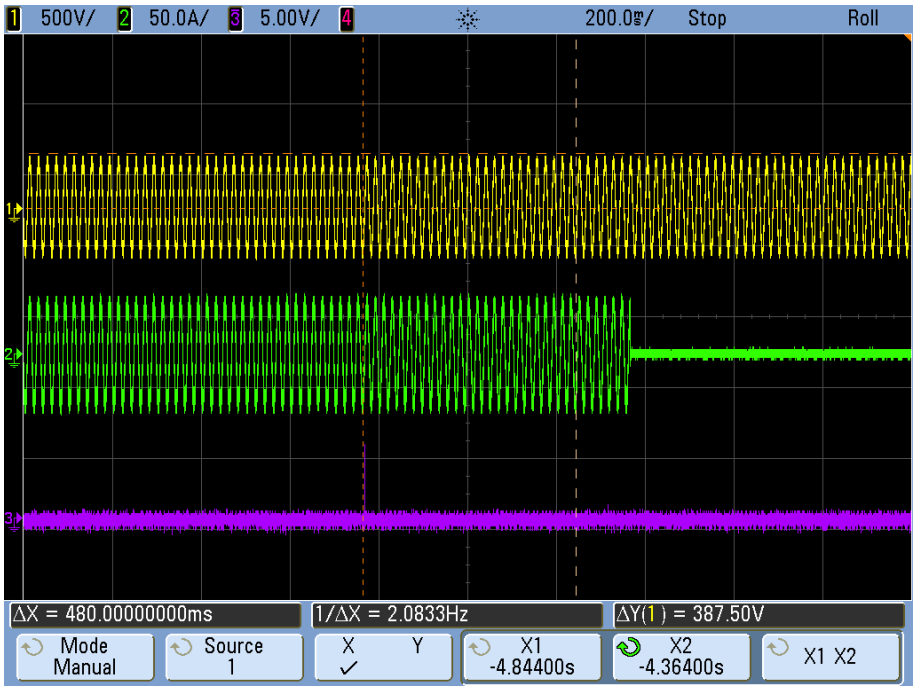
Frequency no-trip tests - Test 4



Appendix 1: Testing table

Frequency no-trip tests - Test 5

Frequency no-trip tests - Test 6



Appendix 1: Testing table

Table 5.3.2 LOSS OF MAINS TEST (The tests carried out in accordance with BS EN 62116									P
No.	**PEUT[1] (% of EUT rating)**	**Reactive load (% of QL in 6.1.d)1)**	**PAC[2] (% of nominal)**	**QAC[3] (% of nominal)**	**Run on time (ms)**	**PEUT (W)**	**Actual Qf**	**VDC**	**Remarks[4]**
1	100	100	0	0	716.0	2.966	1.05	54.82	Test A at BL
2	66	66	0	0	712.2	1.918	1.05	51.45	Test B at BL
3	33	33	0	0	674.0	0.751	0.95	47.32	Test C at BL
4	100	100	-5	-5	416.0	2.944	1.08	54.78	Test A at IB
5	100	100	-5	0	572.0	2.948	1.10	54.72	Test A at IB
6	100	100	-5	5	672.0	2.943	1.13	54.73	Test A at IB
7	100	100	0	-5	626.0	2.944	1.03	54.76	Test A at IB
8	100	100	0	5	424.0	2.950	1.08	54.71	Test A at IB
9	100	100	5	-5	358.0	2.950	1.00	54.71	Test A at IB
10	100	100	5	0	172.0	2.949	1.02	54.72	Test A at IB
11	100	100	5	5	591.0	2.946	1.03	54.82	Test A at IB
12	66	66	0	-5	314.2	1.923	1.03	51.24	Test B at IB
13	66	66	0	-4	608.2	1.927	1.03	51.37	Test B at IB
14	66	66	0	-3	506.2	1.930	1.04	51.36	Test B at IB
15	66	66	0	-2	246.2	1.918	1.04	51.43	Test B at IB
16	66	66	0	-1	696.2	1.919	1.04	51.43	Test B at IB
17	66	66	0	1	718.2	1.930	1.06	51.20	Test B at IB
18	66	66	0	2	662.0	1.918	1.06	51.15	Test B at IB
19	66	66	0	3	514.0	1.925	1.06	51.12	Test B at IB
20	66	66	0	4	780.0	1.921	1.06	51.14	Test B at IB
21	66	66	0	5	368.0	1.923	1.08	51.04	Test B at IB
22	33	33	0	-5	470.0	0.758	0.89	47.29	Test C at IB
23	33	33	0	-4	510.0	0.757	0.90	47.12	Test C at IB
24	33	33	0	-3	562.0	0.758	0.90	47.13	Test C at IB
25	33	33	0	-2	694.0	0.757	0.94	47.14	Test C at IB
26	33	33	0	-1	446.0	0.754	0.94	47.12	Test C at IB
27	33	33	0	1	290.0	0.758	0.95	47.10	Test C at IB
28	33	33	0	2	132.0	0.758	0.95	47.07	Test C at IB
29	33	33	0	3	522.0	0.756	0.96	47.20	Test C at IB
30	33	33	0	4	338.0	0.755	0.96	47.09	Test C at IB
31	33	33	0	5	200.0	0.758	0.96	47.10	Test C at IB

Remark:

1) PEUT: EUT output power
2) PAC: Real power flow at S1 in Figure 1. Positive means power from EUT to utility. Nominal is the 0% test condition value.
3) QAC: Reactive power flow at S1 in Figure 1. Positive means power form EUT to utility. Nominal is the 0% test condition value.
4) BL: Balance condition, IB: Imbalance condition

Appendix 1: Testing table

Table 5.3.3 Protection. Frequency change, Stability test The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6				P
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		No trip
Negative Vector Shift	50.5Hz	- 9 degrees		No trip
Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	No trip
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	No trip

Table 5.3.4 Protection. Re-connection timer. The requirement is specified in section 5.3.4, test procedure in Annex A or B 1.3.5						P
Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1.						
Time delay setting	Measured delay	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.				
65s	78s	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz	
Confirmation that the SSEG does not re-connect.		Not reconnection	Not reconnection	Not reconnection	Not reconnection	

Table 5.4.1 Harmonics						P
SSEG rating per phase (rpp)			3kW		NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output		100% of rated output			
	Measured Value (MV)	Normalised Value (NV)	Measured Value (MV)	Normalised Value (NV)	Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2	0.030	0.037	0.023	0.028	1.080	
3	0.222	0.272	0.223	0.273	2.300	
4	0.013	0.016	0.013	0.017	0.430	
5	0.117	0.144	0.128	0.157	1.140	
6	0.011	0.014	0.010	0.012	0.300	
7	0.070	0.086	0.071	0.087	0.770	

Appendix 1: Testing table

8	0.009	0.011	0.009	0.011	0.230	
9	0.056	0.069	0.060	0.073	0.400	
10	0.007	0.008	0.007	0.009	0.184	
11	0.042	0.052	0.051	0.063	0.330	
12	0.007	0.008	0.006	0.008	0.153	
13	0.038	0.047	0.043	0.053	0.210	
14	0.007	0.008	0.006	0.008	0.131	
15	0.031	0.038	0.035	0.043	0.150	
16	0.029	0.036	0.029	0.035	0.115	
17	0.024	0.030	0.031	0.038	0.132	
18	0.004	0.005	0.004	0.005	0.102	
19	0.022	0.026	0.030	0.037	0.118	
20	0.004	0.005	0.004	0.005	0.092	
21	0.018	0.022	0.028	0.034	0.107	0.160
22	0.004	0.005	0.003	0.004	0.084	
23	0.018	0.022	0.024	0.030	0.098	0.147
24	0.003	0.004	0.003	0.004	0.077	
25	0.013	0.016	0.022	0.027	0.090	0.135

Appendix 1: Testing table

26	0.003	0.003	0.003	0.003	0.071	
27	0.013	0.016	0.022	0.027	0.083	0.124
28	0.003	0.003	0.003	0.003	0.066	
29	0.008	0.010	0.018	0.023	0.078	0.117
30	0.002	0.003	0.002	0.003	0.061	
31	0.007	0.009	0.017	0.021	0.073	0.109
32	0.002	0.003	0.003	0.003	0.058	
33	0.006	0.008	0.016	0.020	0.068	0.102
34	0.002	0.002	0.002	0.002	0.054	
35	0.003	0.004	0.012	0.014	0.064	0.096
36	0.002	0.002	0.002	0.002	0.051	
37	0.002	0.002	0.010	0.012	0.061	0.091
38	0.002	0.002	0.002	0.002	0.048	
39	0.003	0.004	0.014	0.017	0.058	0.087
40	0.002	0.002	0.002	0.002	0.046	

Note:

1. the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.

Appendix 1: Testing table

Power Quality. Voltage fluctuations and Flicker. The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3								
	Starting			Stopping			Running	
	d_{max}	d_c	$d_{(t)}$	d_{max}	d_c	$d_{(t)}$	P_{st}	P_{lt} 2 hours
Measured Values(%)	2.735	0.543	0.000	0.472	0.139	0.000	0.990	0.485
Normalised to standard impedance and 3.68kW for multiple units(%)	100%	100%	100%	100%	100%	100%	100%	100%
Limits set under BS EN 61000-3-2	4%	3.3%	3.3% 500ms	4%	3.3%	3.3% 500ms	1.0	0.65

Table 5.5 and 5.6						P
G83/2 Limit	**DC injection**			**Power factor**		
	0.25%, tested at three power levels Limited: 32.5mA			0.95 lag– 0.95 lead at three voltage levels, Measured at three voltage levels and at full output. Voltage to be maintained within ±1.5% of the stated level during the test.		
Test level	10%	55%	100%	216.2V	230V	253V
Test value	1.1mA	8.4mA	10.1mA	0.9988	0.9988	0.9979

Table 5.7 Fault level contribution. The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6		
For an Inverter SSEG.		
Time after fault	Volts (Peak)	Amps (Peak)
20ms	74.09	7.366A
100ms	48.56	0
250ms	41.78	0
500ms	48.75	0
Time to trip	51.82ms	

SELF MONITORING – SOLID STATE SWITCHING	
Test	YES/NO
It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volt within 0.5 sec.	No (mechanical relays used)

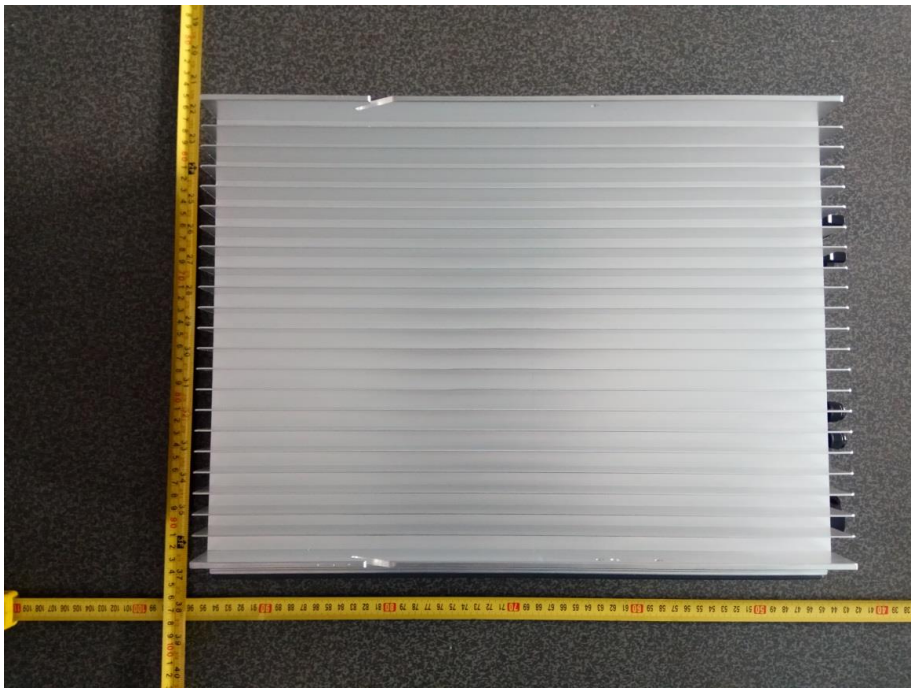
Appendix 2: Photos

Front

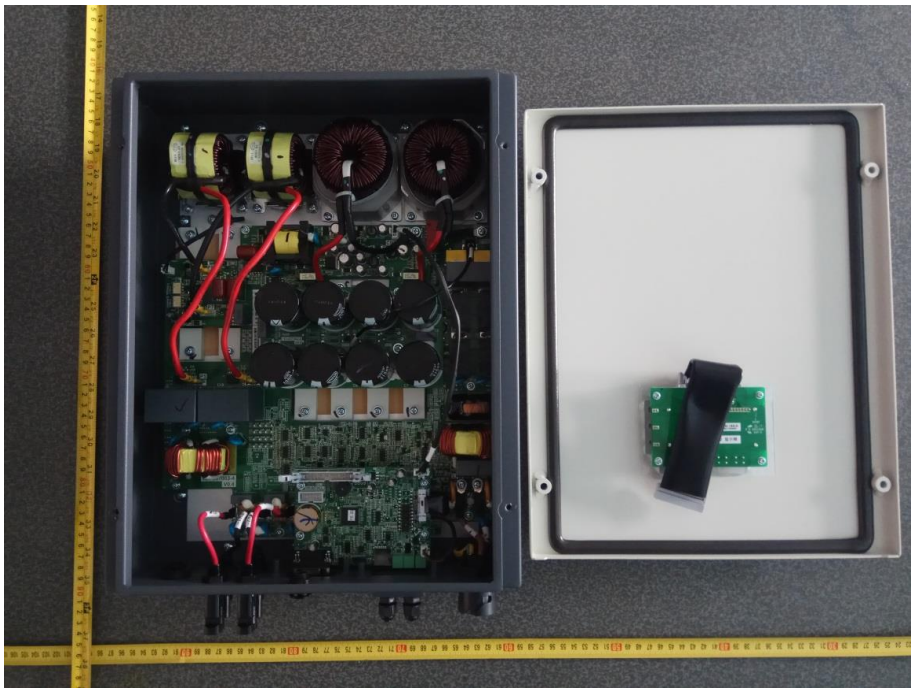
Side


Appendix 2: Photos

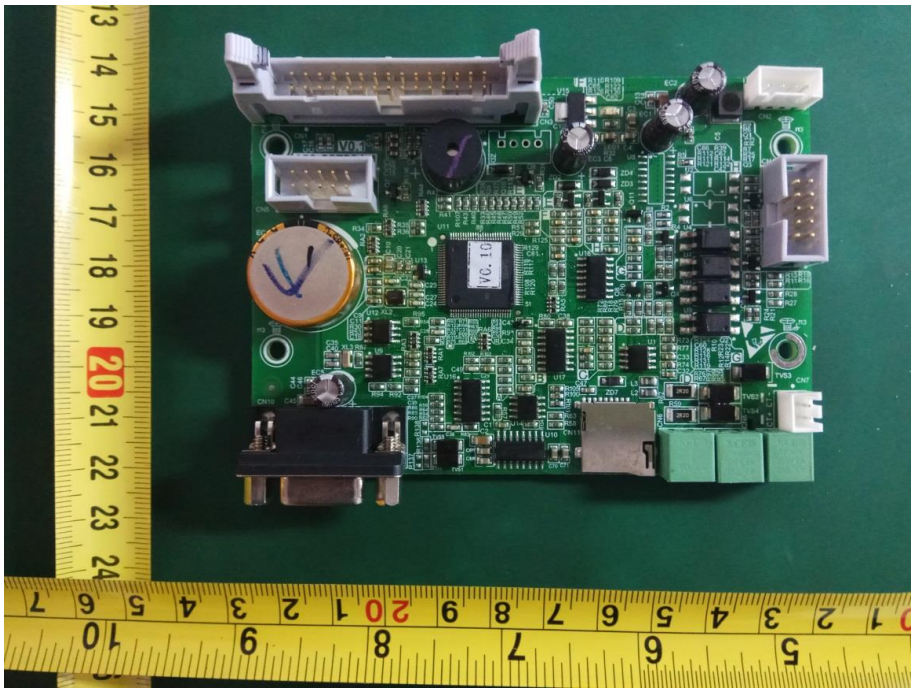
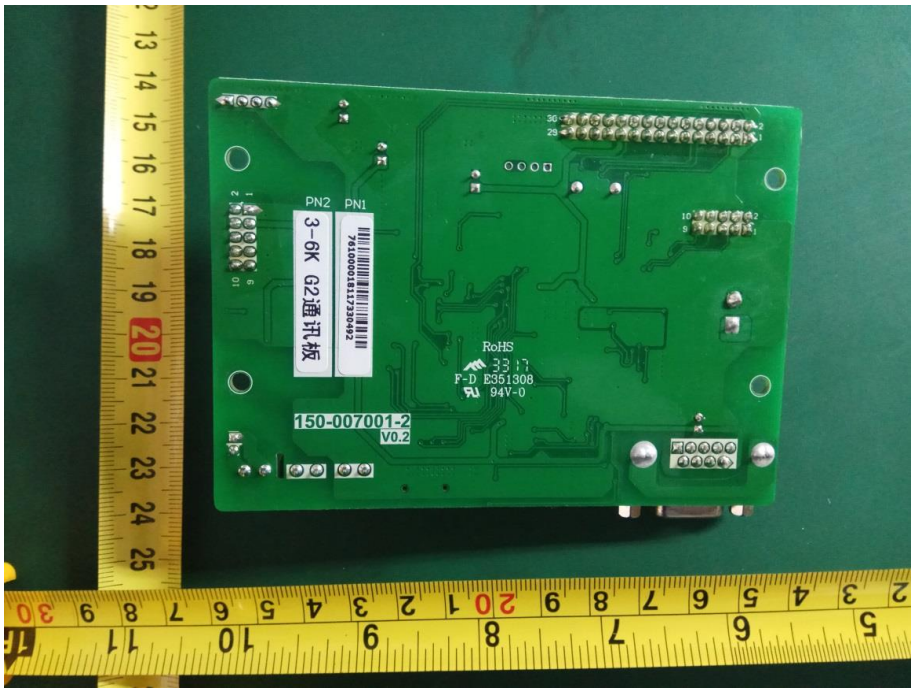
Connection interface

Back Side


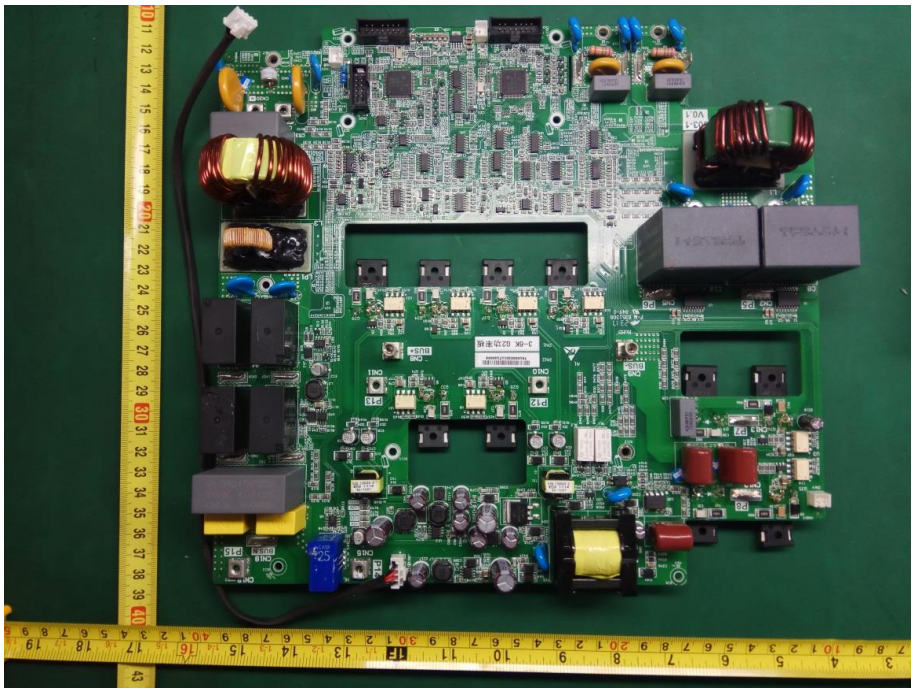
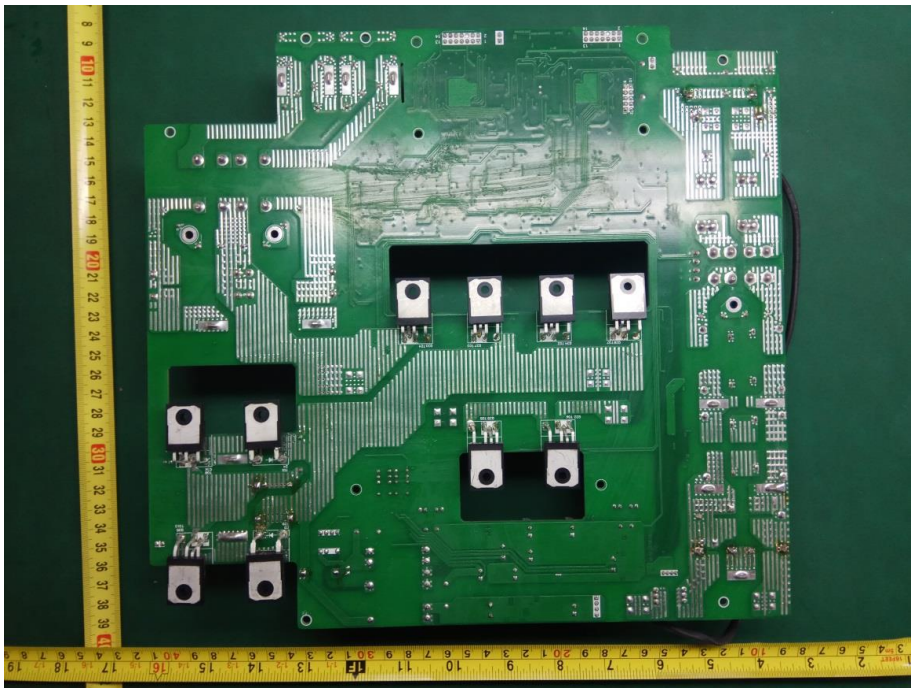
Appendix 2: Photos

Internal

Internal

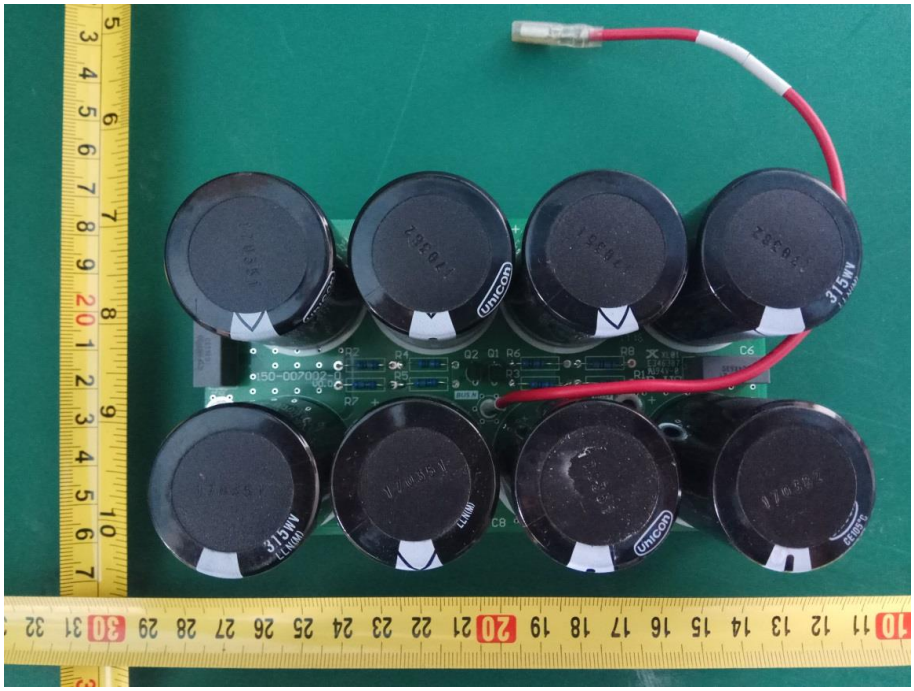
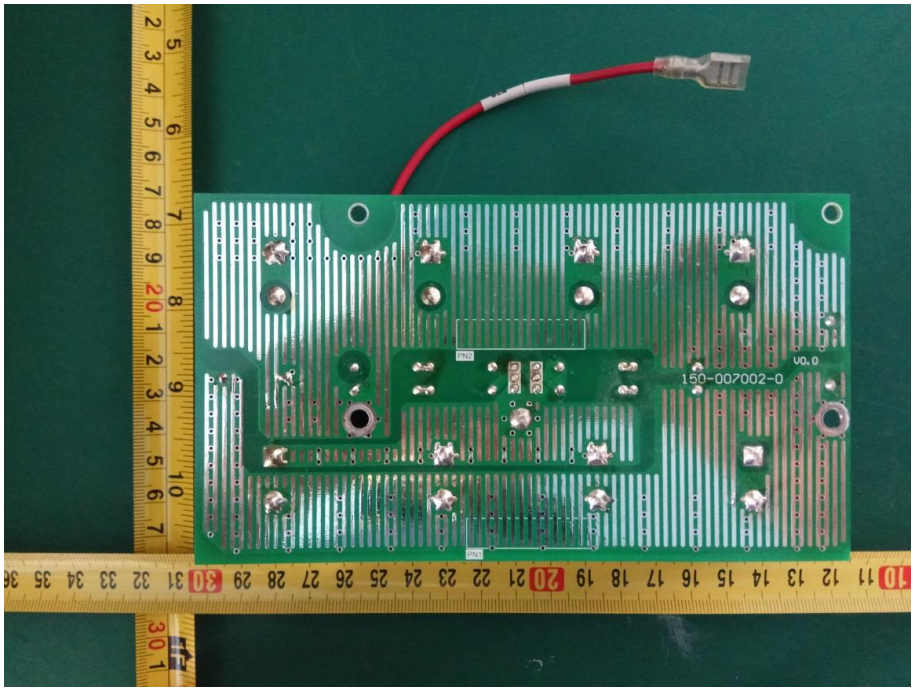

Appendix 2: Photos

Front side of communication baord

Back side of communication baord


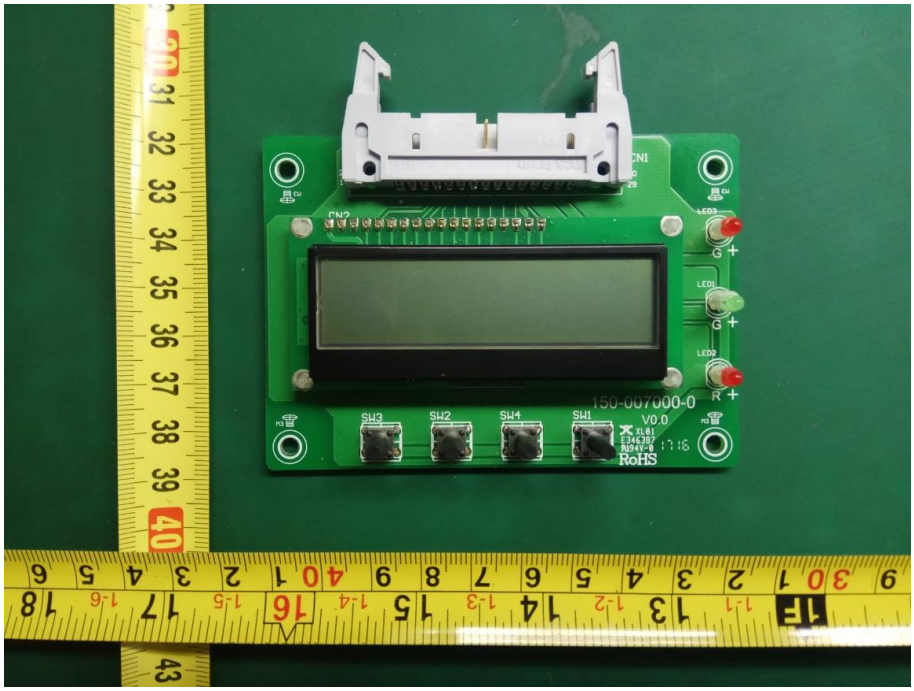
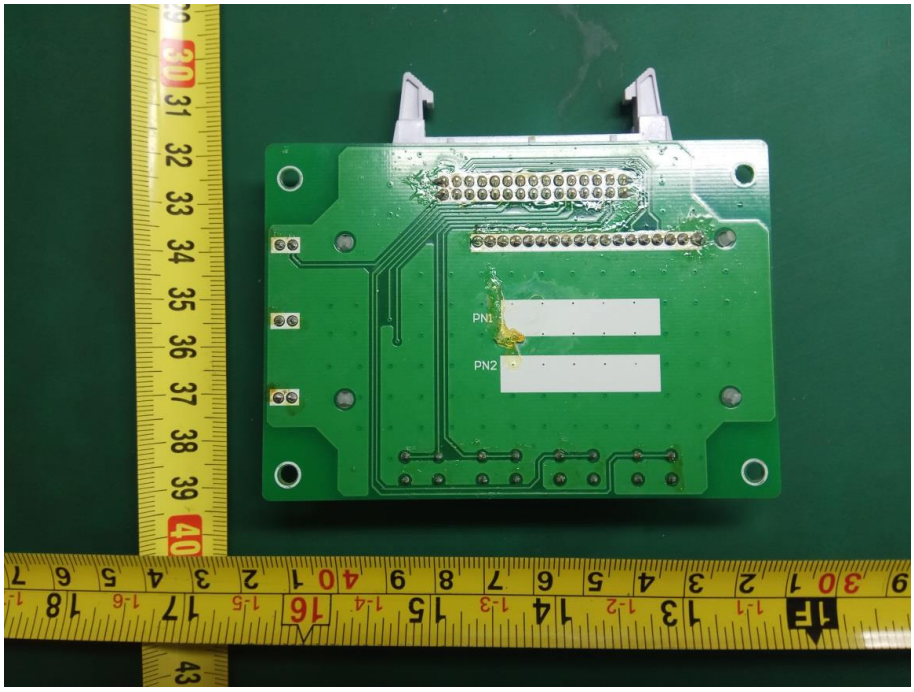
Appendix 2: Photos

Front side of Main board

Front side of Main board


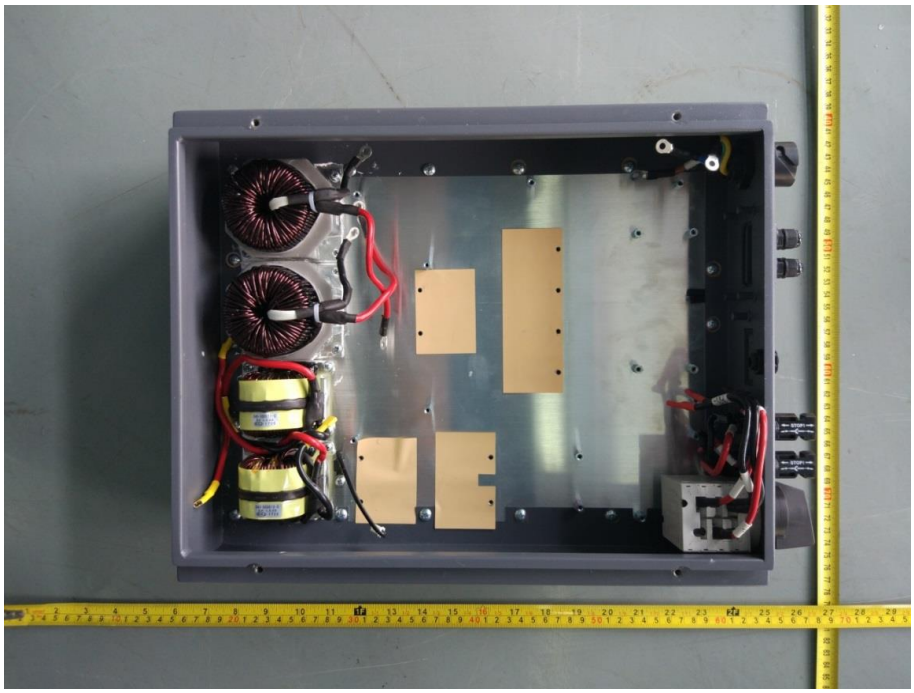
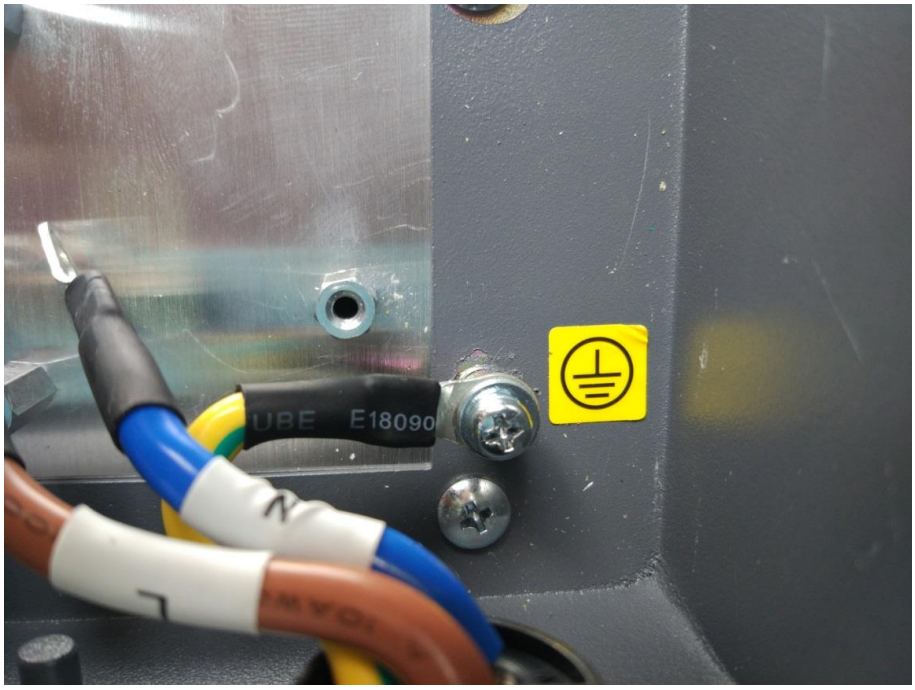
Appendix 2: Photos

Front side of Bus capacitors board

Back side of Bus capacitors board


Appendix 2: Photos

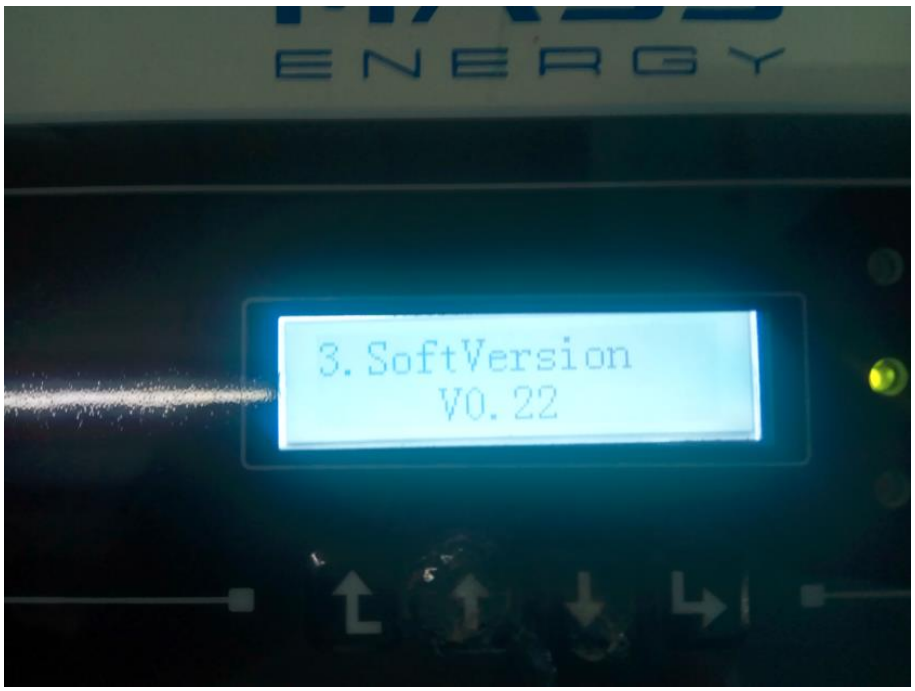
Front side of display board

Back side of display board


Appendix 2: Photos

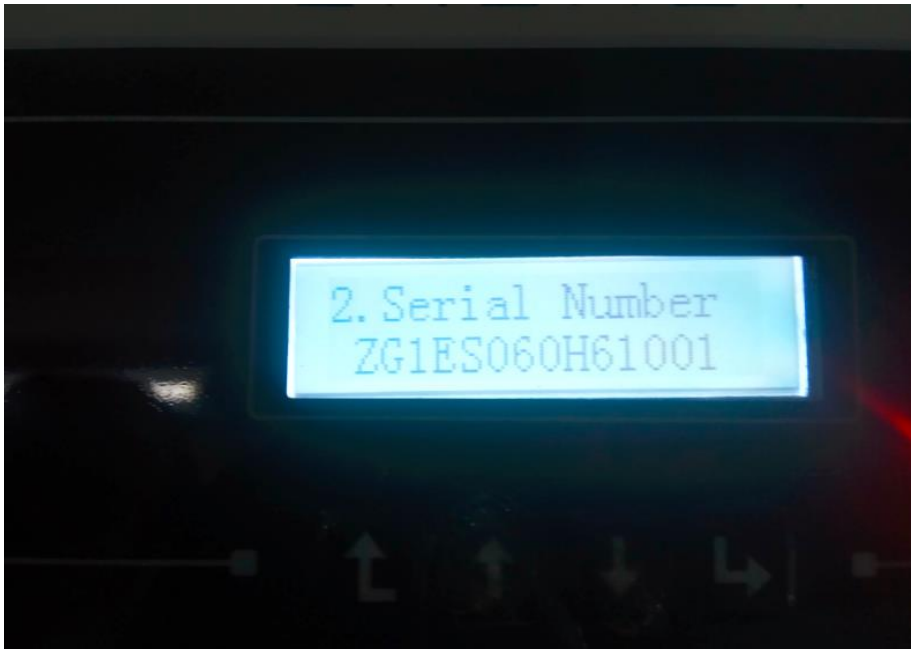
Removed all PCBAs

Cover


Appendix 2: Photos

Labels

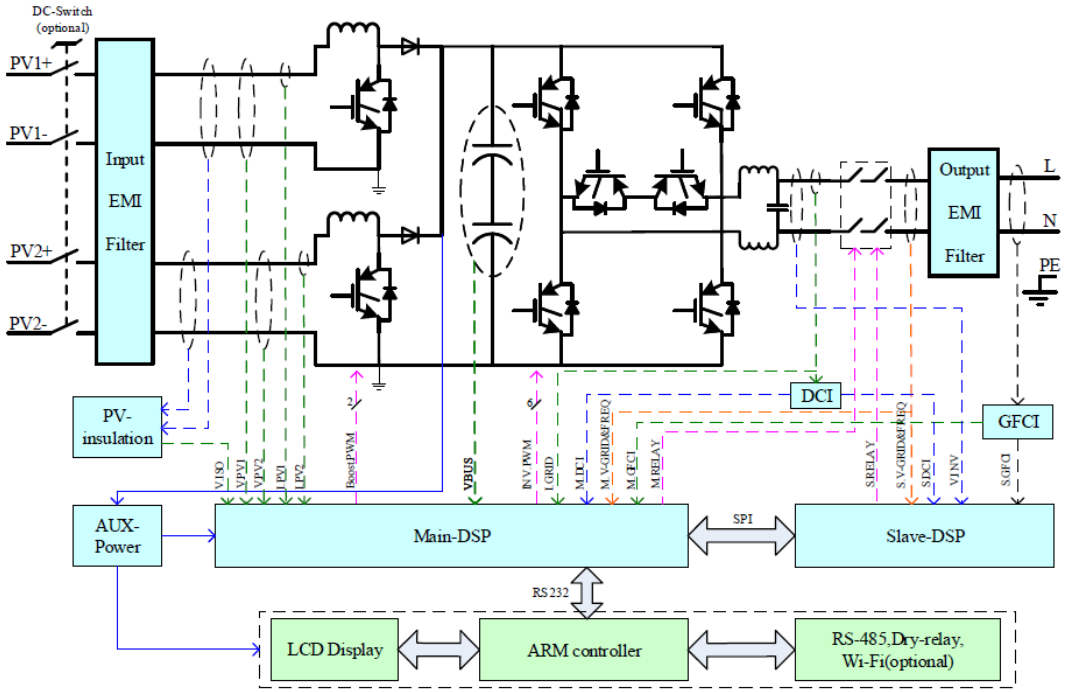
Software Version


Appendix 2: Photos

Serial Number of the EUT


Appendix 3: Electrical Schemes

Equipment under testing



Appendix 4: CE Conformity Certificate

ATTESTATION
of conformity with European Directives

Attestation Number:	1788AB0829N003001
Product:	Solar Inverter
Brand Name:	SOFAR SOLAR
Model:	SOFAR 6KTLM-G2, SOFAR 3KTLM-G2
Additional Model:	SOFAR 5KTLM-G2, SOFAR 4.6KTLM-G2, SOFAR 4KTLM-G2, SOFAR 3.6KTLM-G2
Applicant:	Shenzhen SOFAR SOLAR Co., Ltd.
Address:	5/F,Building 4, Antongda Industrial Park, No.1 Liuxian Avenue,Xin'an Street,Bao'an District, Shenzhen City, Guangdong Province,P.R. China.
Technical Characteristics:	DC input 90-580V AC output 220-230V 50/60Hz

The submitted sample of the above equipment has been tested for CE marking according to following European Directive and following standards:

- Electromagnetic Compatibility Directive 2014/30/EU

Standards	Report Number	Report date
EN 61000-6-3:2007 + A1:2011 EN 61000-3-2:2014 EN 61000-3-3:2013 EN 61000-3-11:2001 EN 61000-3-12:2011 EN 61000-6-2:2005	CE170829N003	Dec. 08, 2017

The referred test report(s) show that the product complies with standard(s) recognized as giving presumption of compliance with the essential requirements in the specified European Directive.

This verification does not imply assessment of the production of the product. The CE marking may be affixed if all relevant and effective European Directives with CE are applicable.

CE

Supervisor
EMC Department

Name: Madison Luo
Date: Dec. 08, 2017

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(End of the report)